DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78220, 78224

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78220 and μPD78224 are products in the 78K/II series single-chip microcomputer.
The μPD78224 has an internal 16K-byte mask ROM and 640-byte RAM.
The μPD78220 is identical to the μPD78224 except that it has no built-in ROM.

Detail functions are described in the following user's manuals. Be sure to read these manuals when desgning your system.

μPD78224 Series User's Manual - Hardware : IEU-5019
78K/II Seires User's Manual - Instruction : IEU-754

FEATURES

- High instruction execution speed (at 12 MHz): 333 ns (μPD78224), 500 ns (μPD78220)
- I/O pins: 63 (μPD78224), 45 (μPD78220)
- Comparator: 4-bit resolution x 8
- Instruction set suitable for control applications
- Data memory expansion function (memory space: 1M bytes)
- High-performance interrupt controller
- High-performance time/counter (16 bits x 1 and 8 bits x 2)
- Serial interface (UART x 1, CSI x 1)
- Real-time output port (8 x 1 or 4 x 2)

APPLICATION FIELD ★

Used in typewriters, portable word processors, electronic cash register and such like to produce alphbet and "kanji" characters.

ORDERING INFORMATION

Part Number	Package Type	Internal ROM	Internal RAM
μPD78220GJ-5BG	94-pin plastic QFP (□ 20 mm)	Not provided	640
μPD78220L	84-pin plastic QFJ (□ 1150 mil)	Not provided	640
μPD78224GJ-XXX-5BG	94-pin plastic QFP (□ 20 mm)	16K	640
μPD78224L-XXX	84-pin plastic QFJ (□ 1150 mil)	16K	640

Remarks: XXX is ROM code number.

QUALITY GRADE

Standard

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and their recommended applications.

Document No. IC-2374D
(O. D. No. IC-5457D)
Date Published January 1994 P
Printed in Japan

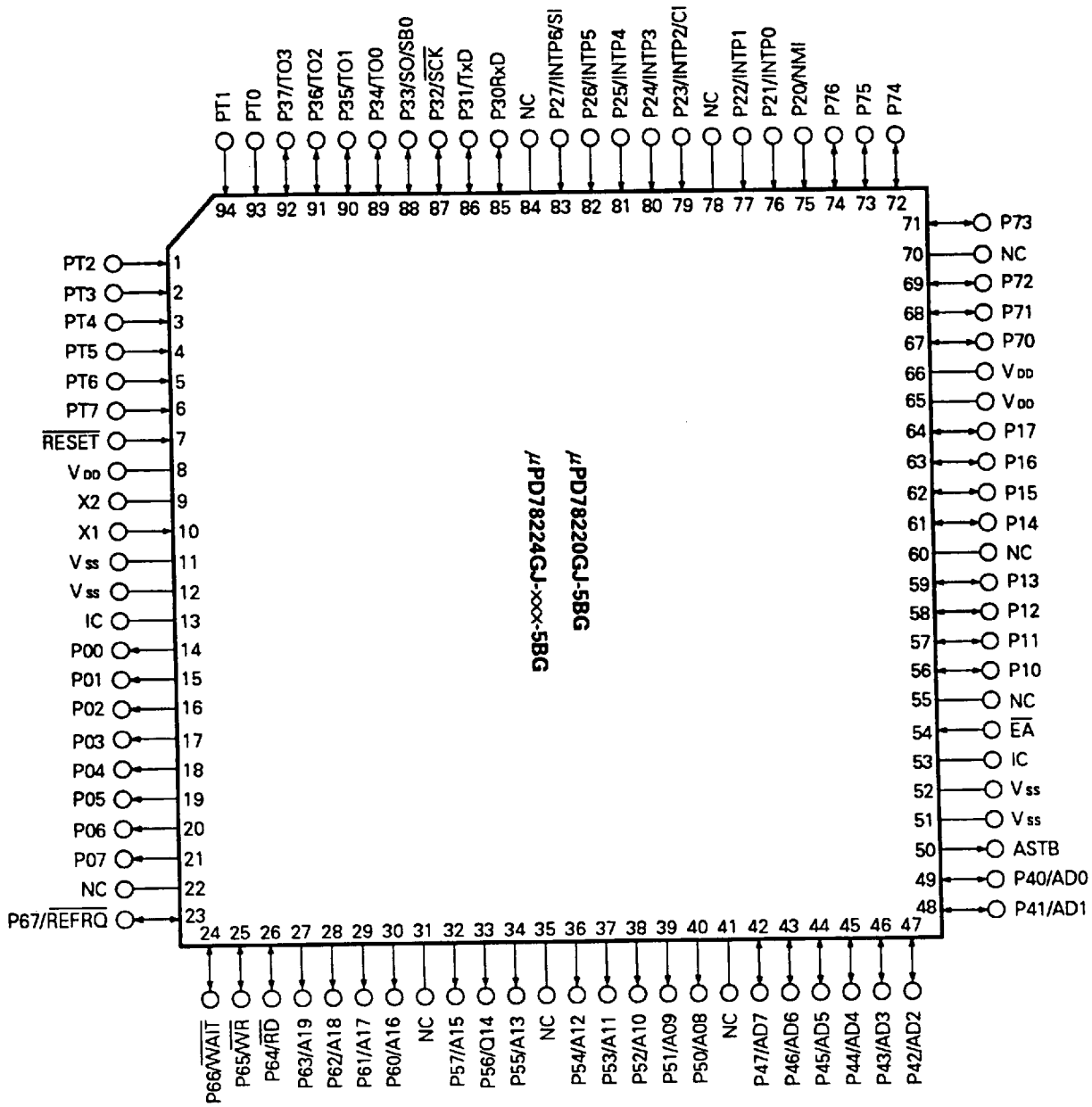
The mark ★ shows major revised points.

FUNCTIONAL LIST

Item	Contents
Number of Instructions (mnemonic)	65
Minimum Instruction-Execution Time	• 333ns at 12MHz (μPD78224) • 500ns at 12MHz (μPD78220)
Internal Memory	• ROM: 16k bytes (μPD78224 only) • RAM: 640 bytes
Address Space	• Program memory space: 64K bytes • Data memory space: 1M bytes
General-Purpose Register	8 bits × 8 × 4 banks (memory mapped)
I/O Pins	71 total • Input port pins: 8 • Output port pins: 20 • Input/output port pins: 35 (Of these 20, 8 are capable of directly drive LEDs) • With comparator: 8
Timer/Counter	• 16-bit timer/counter { Timer register × 1; Capture register × 1; Compare register × 2 } Pulse output (toggle output)
	• 8-bit timer/counter 1 { Timer register × 1; Capture/compare register × 1; Compare register × 1 } Pulse output (real-time output: 4 bits x 2)
	• 8-bit timer/counter 2 { Timer register × 1; Capture register × 1; Compare register × 2 } Pulse output (toggle output)
Serial Interface	• UART: 1 channel • CSI (3-line serial I/O, SBI): 1 channel • Exclusive internal baud rate generator
Interrupts	• 17 interrupt sources (External: 8, Internal: 9) + BRK instruction • Two priority levels (programmable) • Two interrupt-handling modes (Vector interrupt/macro service)
Stand-By	HALT/STOP mode
Instruction Set	• 16-bit arithmetic • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation • BCD adjust, others
Inputs with Comparator	4-bit resolution, variable threshold level
Real-Time Output Ports	Port output function interlocked with the internal timer • Two 4-bit channels or one 8-bit × 1 channel
Other	Pseudo-static RAM refresh function
Package	• 84-pin plastic QFJ (□1150 mil) • 94-pin plastic QFP (□20 mm)

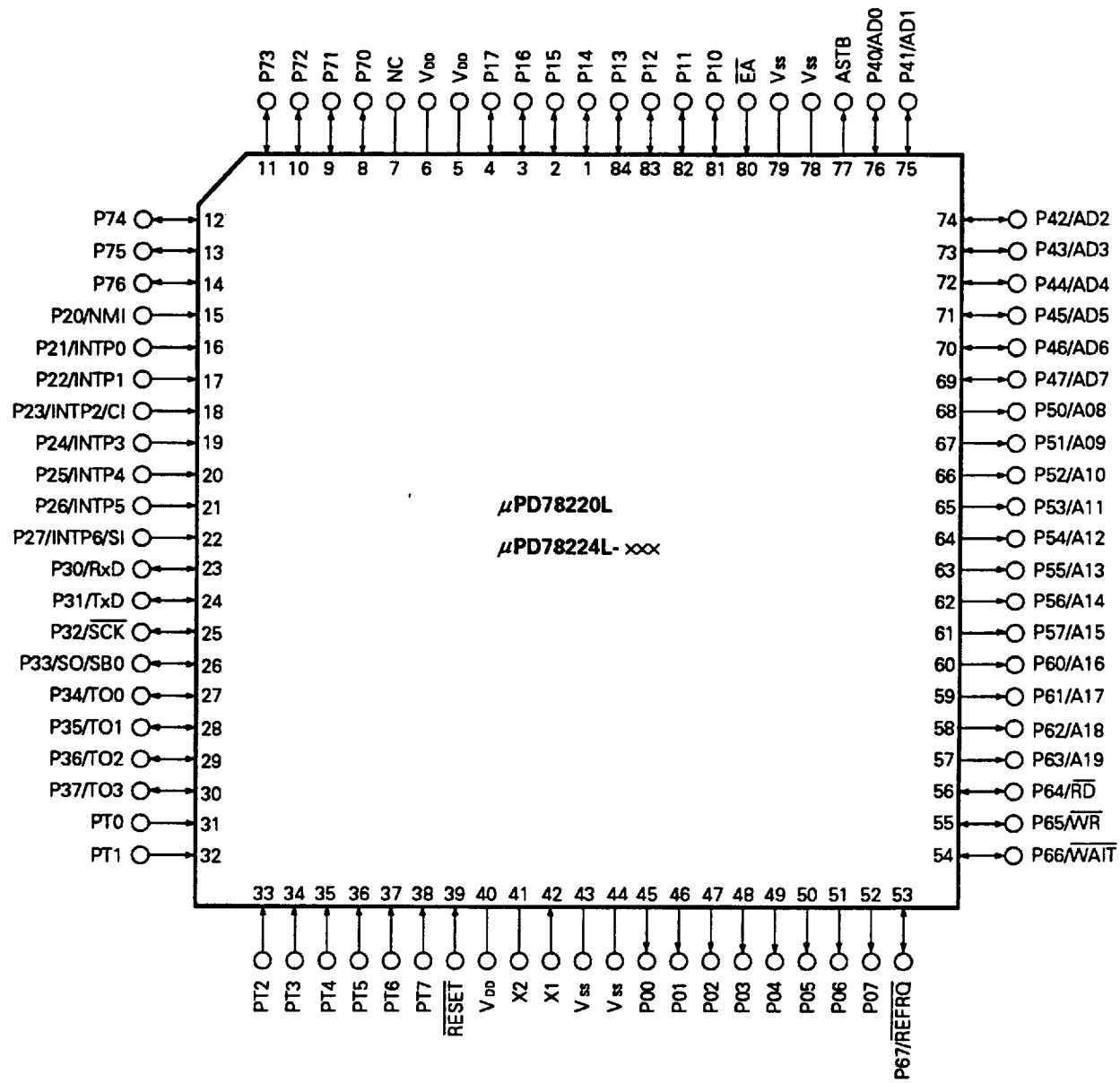
PIN CONFIGURATION (Top View)

94-Pin Plastic QFP (□20 mm)



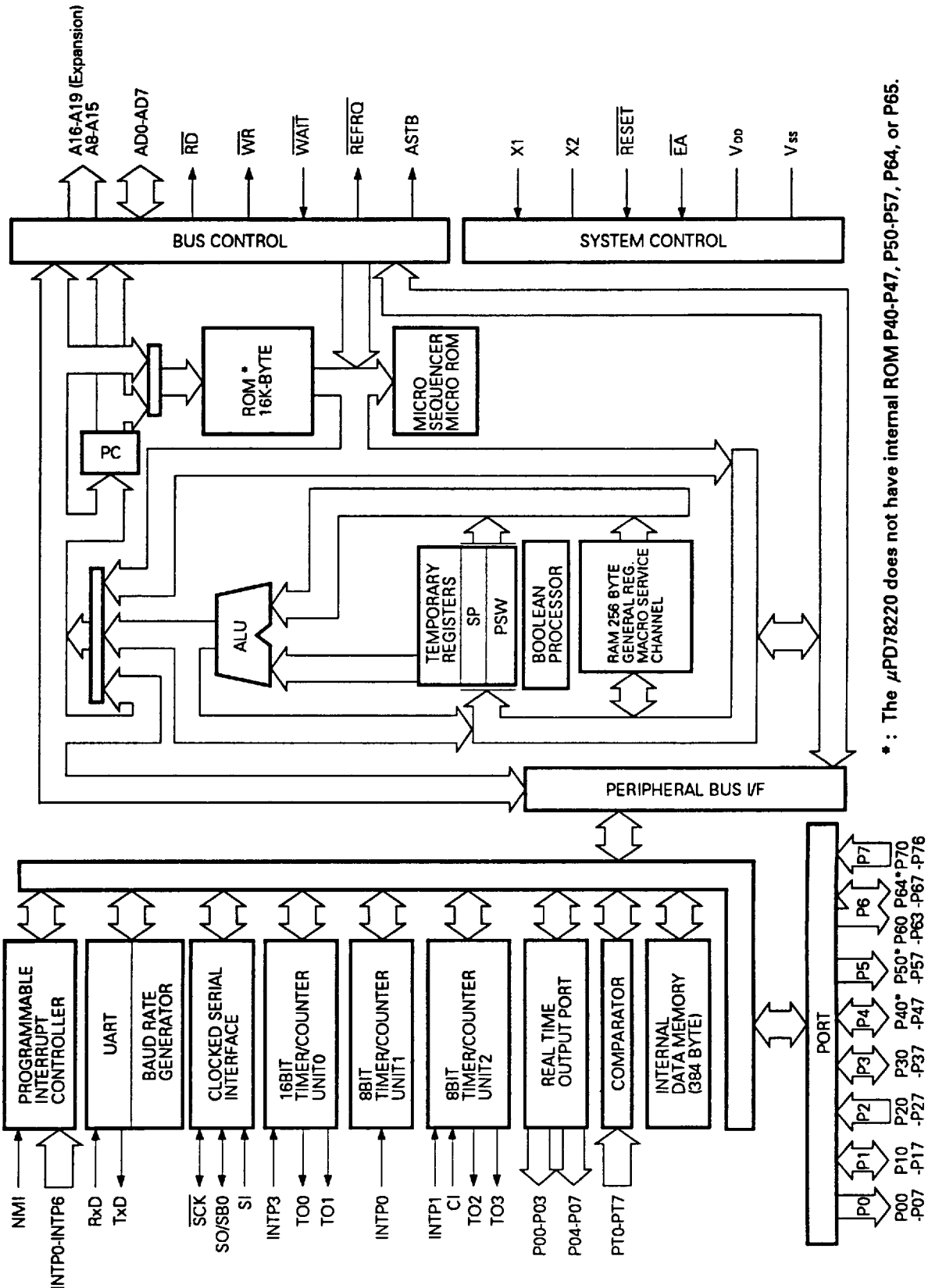
Note : IC pin should be connected directly to Vss(GND).

84-Pin Plastic QFJ (□ 1150 mil)



P00-P07	:	Port 0
P10-P17	:	Port 1
P20-P27	:	Port 2
P30-P37	:	Port 3
P40-P47	:	Port 4
P50-P57	:	Port 5
P60-P67	:	Port 6
P70-P76	:	Port 7
PT0-PT7	:	Port T
TO0-TO3	:	Timer Output
CI	:	Clock Input
RxD	:	Receive Data
TxD	:	Transmit Data
$\overline{SCK}$	:	Serial Clock
SB0	:	Serial Bus
SI	:	Serial Input
SO	:	Serial Output
NMI	:	Nonmaskable Interrupt
INTP0-INTP6	:	Interrupt From Peripherals
AD0-AD7	:	Address Data Bus
A08-A15, A16-A19	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
$\overline{EA}$	:	External Access
X1, X2	:	Crystal
$\overline{REFRQ}$	:	Refresh Request
$\overline{RESET}$	:	Reset
NC	:	Non-connection
IC	:	Internally Connected

μPD78220/μPD78224 BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS

Pin Name	Input/Output	Shared Pin	Function
P00-P07	Output	—	(Port 0) An 8-bit output-only port (P0). This port can also be used as an 8-bit real-time output port or as two 4-bit real-time output ports.
P10-P17	Input/Output	—	(Port 1) An 8-bit input/output port (P1). This port can be specified for input/output in bit units and can drive LEDs.
P20	Input	NMI	(Port 2) An 8-bit input-only port (P2).
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24-P26		INTP3-INTP5	
P27		INTP6/SI	
P30	Input/Output	RxD	(Port 3) An 8-bit input/output port (P3). This port can be specified for input/output in bit units.
P31		TxD	
P32		$\overline{SCK}$	
P33		SO/SB0	
P34-P37		TO0-TO3	
P40-P47	Input/Output	AD0-AD7	(Port 4) An 8-bit input/output port (P4). This port can be specified for input/output in 8-bit units*1.
P50-P57	Output	A08-A15	(Port 5) An 8-bit output-only port (P5)*1.
P60-P63	Output	A16-A19	(Port 6) An 8-bit input/output port (P6). P60-P63 are output only. P64-P67 can be specified for input/output in bit units*2.
P64	Input/Output	$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		$\overline{REFRQ}$	
P70-P76	Input/Output	—	(Port 7) A 7-bit input/output port (P7). This port can be specified for input/output in bit units.
PT0-PT7	Input	—	(Port T) An 8-bit input-only port with comparator (PT).

*1 : These pins of the μPD78220 cannot be used as port pins.

*2 : P64 and P65 of the μPD78220 cannot be used as port pins.

1.2 ALL OTHER PINS

Pin Name	Input/Output	Shared Pin	Function
TO0-TO3	Output	P34-P37	Timer output pin.
CI	Input	P23/INTP2	8-bit timer/counter No. 2 external clock input pin.
RxD	Input	P30	Serial data input pin (UART).
TxD	Output	P31	Serial data output pin (UART).
$\overline{SCK}$	Output	P32	Serial clock input/output pin (SBI, 3-line serial I/O mode).
SB0	Input/Output	P33/SO	Serial data input/output pin (SBI mode).
SI	Input	P27/INTP6	Serial data input pin (3-line serial I/O mode).
SO	Output	P33/SB0	Serial data output pin (3-line serial I/O mode).
NMI	Input	P20	Non-maskable interrupt request input pin for which the rising or falling edge can be specified as the detection edge by the mode register.
INTP0	Input	P21	External interrupt request input pin for which the effective edge can be specified by the mode register.
INTP1		P22	
INTP2		P23/CI	
INTP3-INTP5		P24-P26	
INTP6		P27/SI	
AD0-AD7	Input/Output	P40-P47*	Time-division multiplexed address/data bus (when the external memory is connected).
A08-A15	Output	P50-P57*	Address output port (when the external memory is connected).
A16-A19	Output	P60-P63	Upper address output pin (when the external memory is expanded).
$\overline{RD}$	Output	P64*	Strobe signal output pin for external memory read operation.
$\overline{WR}$	Output	P65*	Strobe signal output pin for external memory write operation.
$\overline{WAIT}$	Input	P66	Wait signal input pin.
ASTB	Output	—	This pin outputs a timing signal to externally latch the address information for accessing the external memory.
$\overline{EA}$	Input	—	Normally, the $\overline{EA}$ pin is set to 1 (high). When the $\overline{EA}$ pin is set to 0 (low), the ROM-less mode is initiated, and the external memory is accessed.
X1, X2		—	A crystal for the system clock is connected across these pins. The X1 pin is used to input the external clock.
$\overline{REFRQ}$	Output	P67	When a pseudo-static memory is externally connected, this pin is used to output the refresh pulse to the pseudo-static memory.
$\overline{RESET}$	Input	—	Low-level-active system reset input pin.
V_{DD}		—	Positive power supply pin
Vss		—	GND
NC		—	Not internally connected
IC		—	Internal connection pin. Connect this pin directly to Vss (GND).

*: These pins of the μPD78220 cannot be used as port pins.

1.3 PIN INPUT/OUTPUT CIRCUITS AND PROCESSING OF UNUSED PINS

Fig. 1-1 shows the simplified pin input/output circuits of the μPD78224/μPD78220.

Table 1-1 indicates the pin input/output circuit type for each pin.

Table 1-1 Pins and Corresponding Input/Output Circuit Type

Pin	Input/Output Type	I/O	Recommended Connection When Unused
P00-P07	4	Output	Open
P10-P17	5	I/O	Input: Connect to V_{DD} or Vss Output: Open
P20/NMI	2	Input	Connect to V_{DD} or Vss
P21/INTP0			
P22/INTP1			
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK			
P26/INTP5			
P27/INTP6/SI			
P30/RxD	5	I/O	Input: Connect to V_{DD} or Vss Output: Open
P31/TxD			
P32/$\overline{SCK}$	8		
P33/SB0/SO	10		
P34/TO0-P37/TO3	5		
P40/AD0-P47/AD7			
P50/A8-P57/A15			
P60/A16-P63-A19	4	Output	Open
P64/$\overline{RD}$	5	I/O	Input: Connect to V_{DD} or Vss Output: Open
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/$\overline{REFRQ}$			
P70-P76			
PT0-PT7	7-A	Input	Connect to V_{DD}
ASTB	4	Output	Open
$\overline{RESET}$	2	Input	—
$\overline{EA}$	1		
V_{DD}	—	—	Connect to V_{DD}

★ **Note:** If the input or output mode of an input/output pins is undefined, connect the pin to V_{DD} via a resistor with several 10 kΩ of resistance (especially when the voltage on the reset input pin exceeds the input level on power application or when the input or output mode is selected through software).

Remarks: I/O type No. is a serial No. for the 78K series products. It may not be serial in each product (some may not be included).

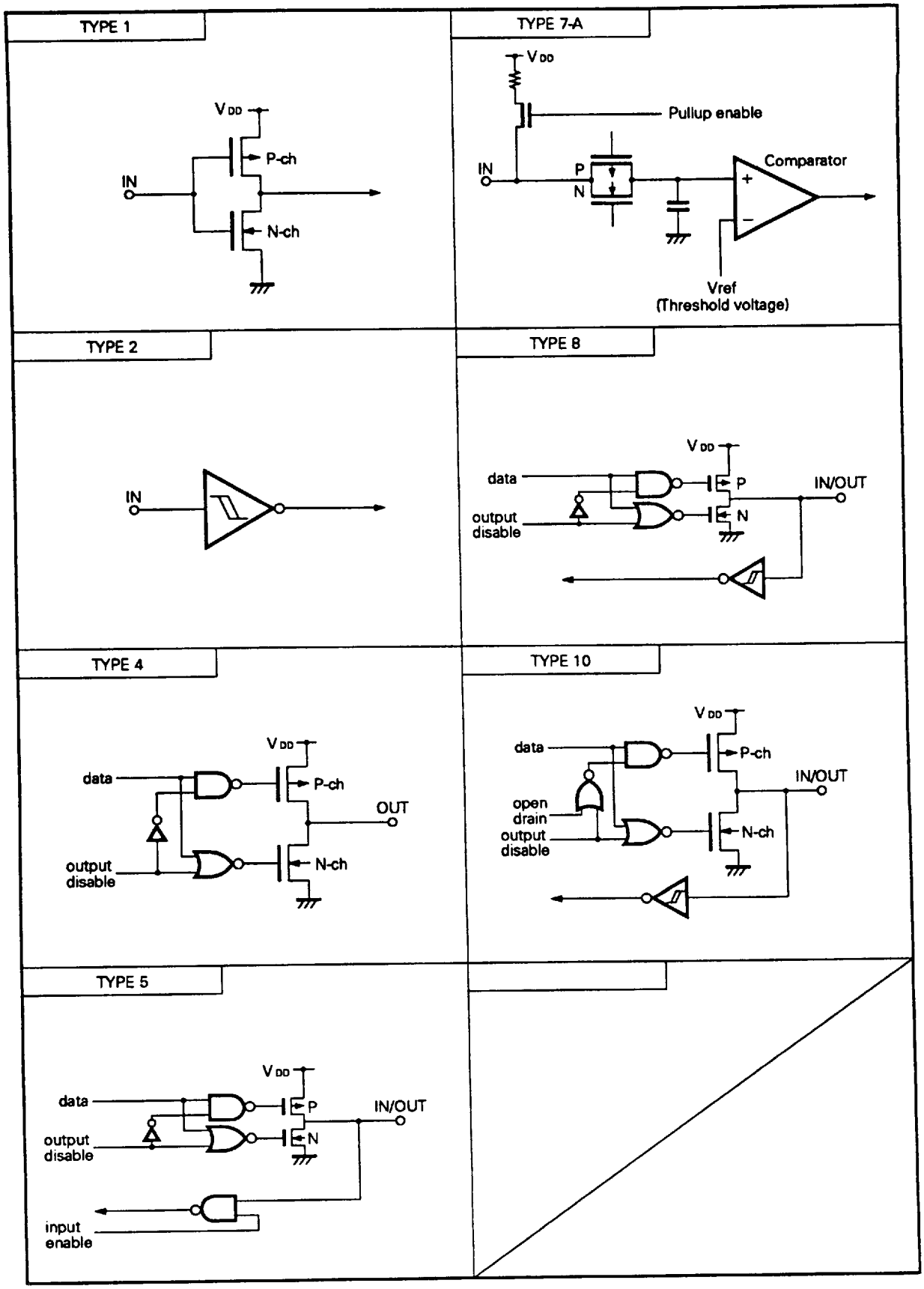


Fig. 1-1 Pin Input/Output Circuits

2. INTERNAL BLOCK FUNCTIONS

2.1 MEMORY SPACE

The μPD78220 and μPD78224 can access a memory space of 1M bytes. Figure 2-1 shows the memory space. The program memory is mapped differently depending on the status of the $\overline{EA}$ pin.

(1) μPD78220 or μPD78224 ($\overline{EA}$ = L)

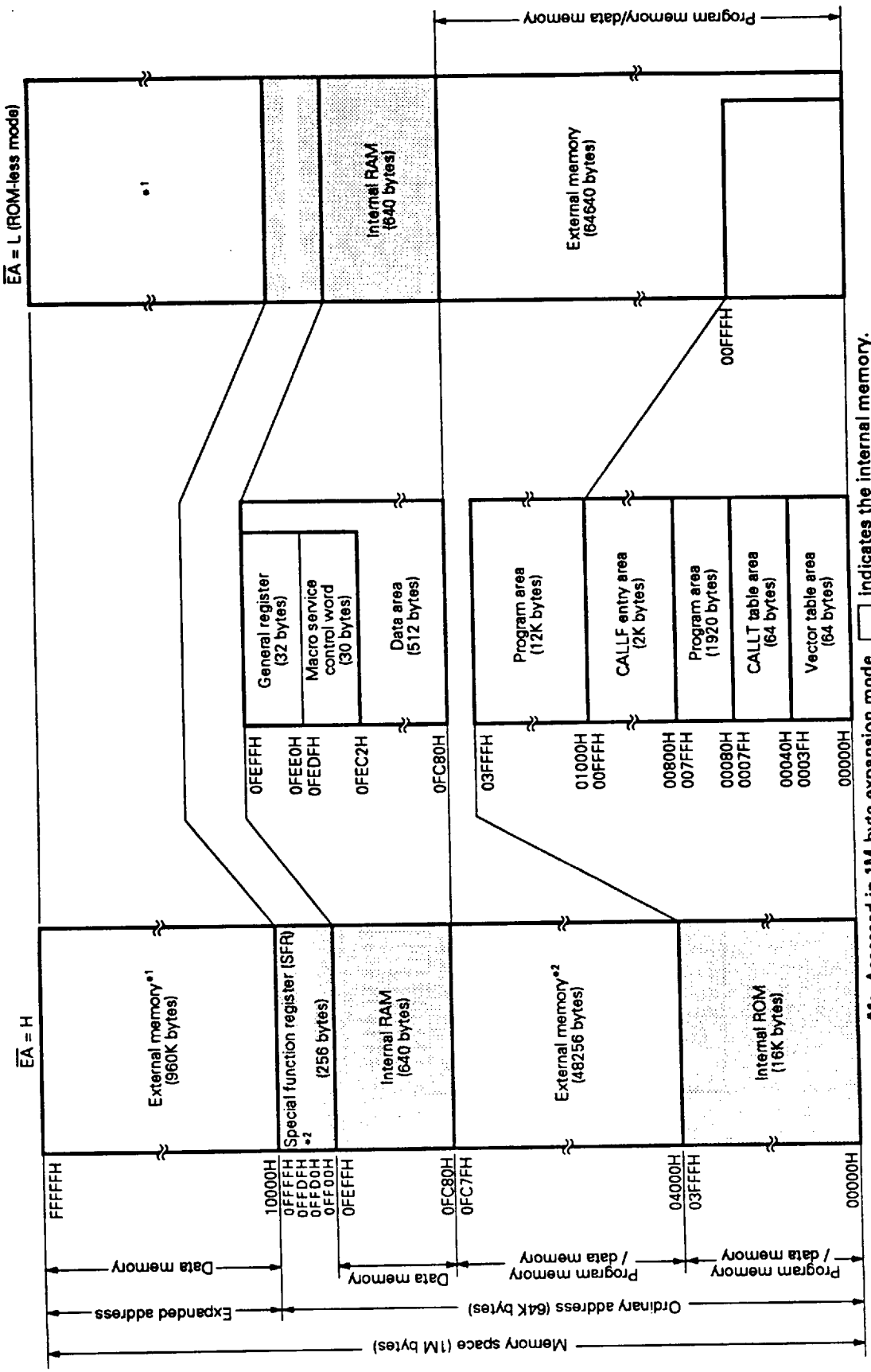
The program memory is mapped to an external memory (64640 bytes: 00000H-0FC7FH). This area can be also shared with the data memory.

The data memory is mapped to the internal RAM (640 bytes: 0FC80H-0FEFFH). In the 1M-byte expansion mode, an external memory (960K bytes: 10000H-FFFFFH) is mapped as an external data memory.

(2) μPD78224 ($\overline{EA}$ = H)

The program memory is mapped to the internal ROM (16K bytes: 00000H-03FFFH) and an external memory (48256 bytes: 04000H-0FC7FH). The external memory is accessed in the external memory expansion mode. The area mapped to the external memory can be shared with the data memory.

The data memory is mapped to the internal RAM (640 bytes: 0FC80H-0FEFFH). In the 1M-byte expansion mode, an external memory (960K bytes: 10000H-FFFFFH) is mapped as an expansion data memory.



*1: Accessed in 1M-byte expansion mode. ☐ indicates the internal memory.
*2: Accessed in external memory expansion mode.
*3: Only when $\overline{EA}$ = L with μPD78220

Fig. 2-1 Memory Map

2.2 PORT FUNCTIONS

2.2.1 Digital Input/Output Ports

The μPD78220/μPD78224 has ports as shown in Fig. 2-2 for a variety of control applications. The functions of each port are shown in Table 2-1.

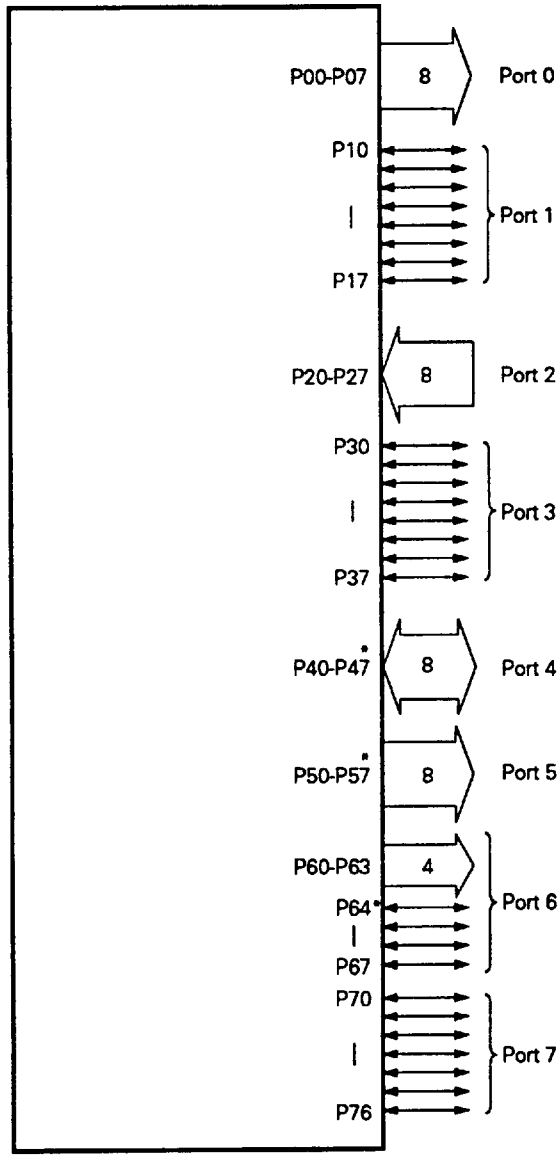


Fig. 2-2 Port Configuration

*: When expanding the external memory or I/O device, pins P40 to P47 serve as the multiplexed address /data bus (AD0 to AD7), pins P50 to P57 as the address bus (A8 to A15), and pins P64 and P65 as the $\overline{RD}$ and $\overline{WR}$ signal outputs, respectively.
These pins of the μPD78220 cannot be used as port pins.

Table 2-1 Features and Functions of Each Port

Port Name	Function	Operation and Features	Remarks
Port 0	8-bit output	This port can be specified either for output or the high impedance state in 8-bit units. P00-P03 and P04-P07 can be used as two independent 4-bit real-time output ports, or P00 to P07 can be used together as a single 8-bit real-time output port.	—
Port 1	8-bit input/output	This port can be specified for input or output in bit units. This port is capable of directly driving LEDs (large current output port).	—
Port 2	8-bit input	This is an input-only port (the pin level can be read). The pins in this port also serve as interrupt input pins. Pins in this port can be used either as control pins or interrupt input pins.	Shared with the NMI, INTP0-INTP6, CI, and SI pins.
Port 3	8-bit input/output	This port can be specified for input or output in bit units. In addition, the pins in this port can be specified as various control pins.	Shared with the RxD, TxD, $\overline{SCK}$, SO/SB0, and AD0-AD7 pins.
Port 4*	8-bit input/output	This port can be specified for input or output in 8-bit units. In addition, this port functions as the time-division multiplexed address/data bus (AD0-AD7) when the external memory or I/O is expanded.	Shared with the AD0-AD7 pins.
Port 5*	8-bit output	This port can be specified either for output or the high impedance state in 8-bit units. In addition, this port functions as the address bus (A08-A15) when the external memory or the I/O requirements are expanded.	Shared with the A08-A15 pins.
Port 6*	8-bit input/output	P60-P63 are output only pins. P64-P67 can be specified for input or output in bit units. The pins of this port can also be used as various control pins.	Shared with the A16-A19, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and $\overline{REFRQ}$ pins.
Port 7	7-bit input/output	This port can be specified for input or output in bit units.	—

*: P40-P47, P50-P57, P64, and P65 of the μPD78220 cannot be used as port pins.

2.2.2 Port T

The μPD78220/μPD78224 has an 8-bit input port with a variable threshold voltage function (Port T), in addition to having digital input/output ports. Fig. 2-3 shows the configuration of Port T.

The threshold voltage of Port T can be selected from among 15 levels (V_{DD} x 1/16 to V_{DD} x 15/16).

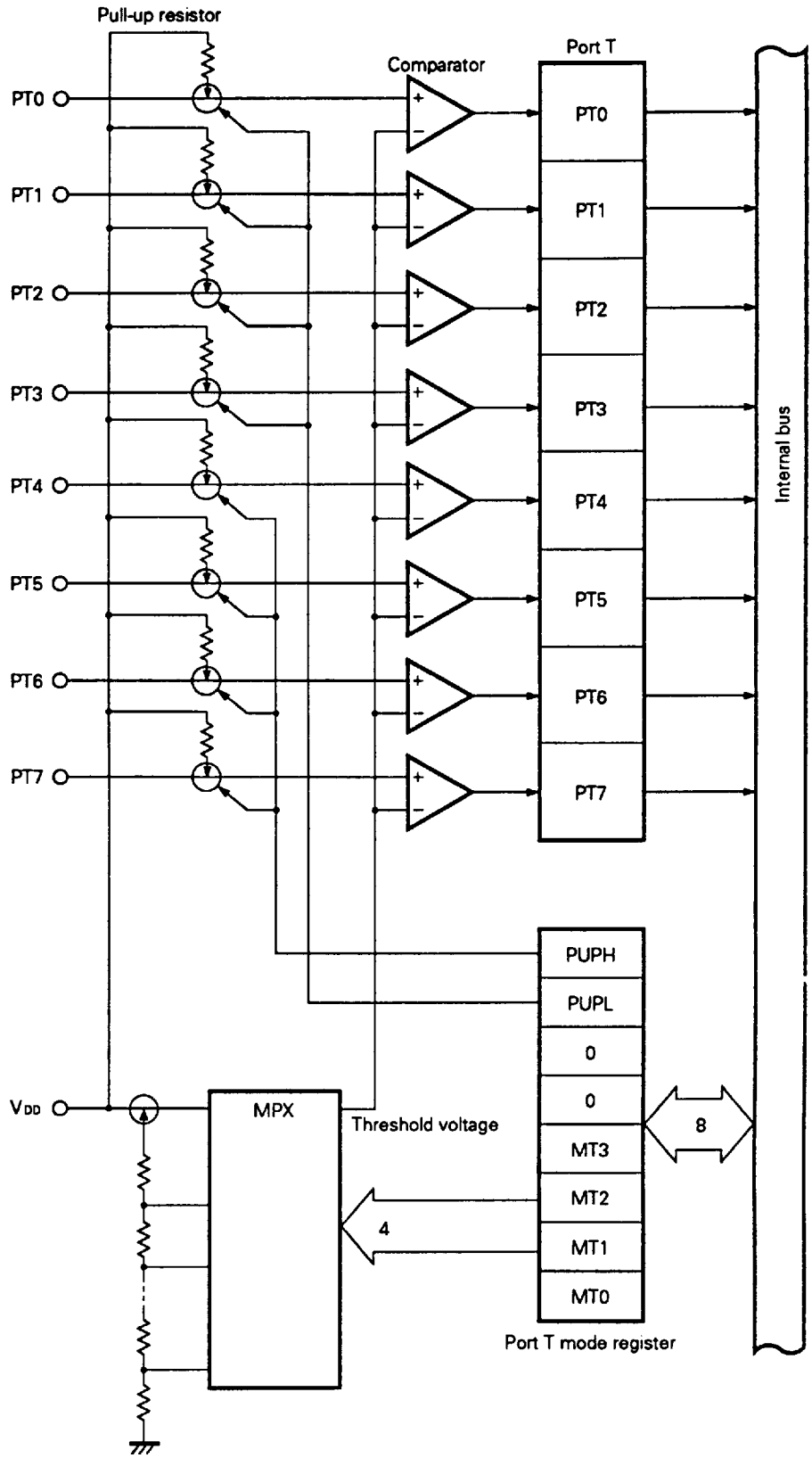


Fig. 2-3 Port T Block Diagram

2.3 REAL-TIME OUTPUT PORT

As shown in Fig. 2-4, the real-time output port consists mainly of Port 0 and buffer register.

By transferring the data stored in the buffer register in advance to the output latch by hardware when the "time coincidence interrupt" or an external interrupt is generated, a jitter-free pulse output can be obtained. The real-time output port is therefore, suitable for applications which require the outputting of an arbitrary pattern with an arbitrary interval, such as for open-loop control of stepping motors.

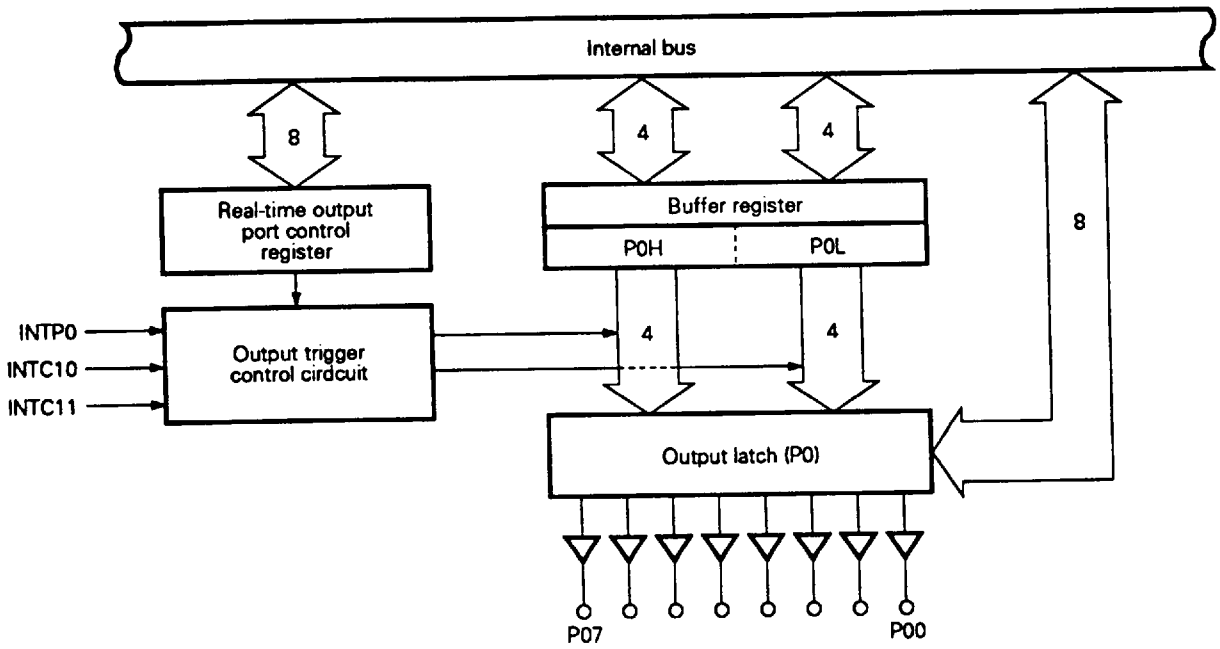


Fig. 2-4 Real-Time Output Port Block Diagram

2.4 TIMER/COUNTER UNIT

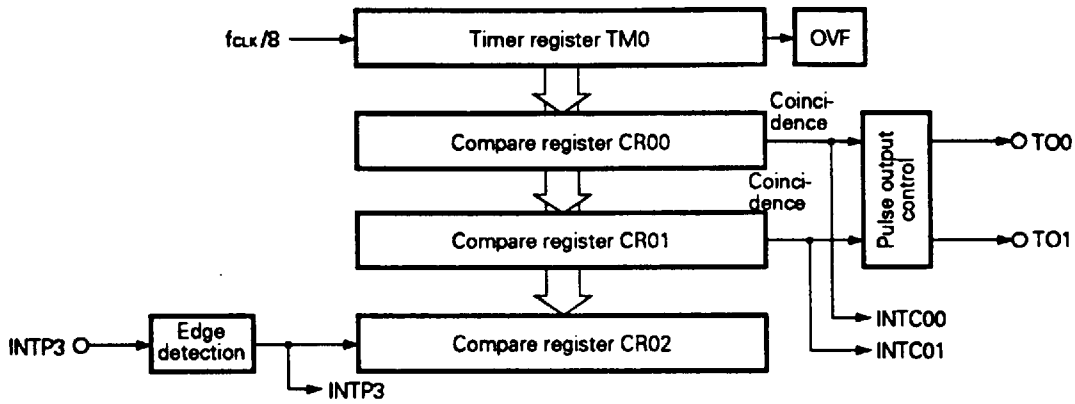
As shown in Fig. 2-4, the μPD78220/μPD78224 has one 16-bit timer/counter channel and two 8-bit time/counter channels. In addition to that, each timer has two or more compare registers. Therefore, the 16-bit timer/counter can perform functions equivalent to a two-channel 16-bit timer/counter, and the two 8-bit timer/counter channels can perform functions equivalent to four 8-bit timer/counters channels.

Table 2-2 lists the functions of each timer/counter unit.

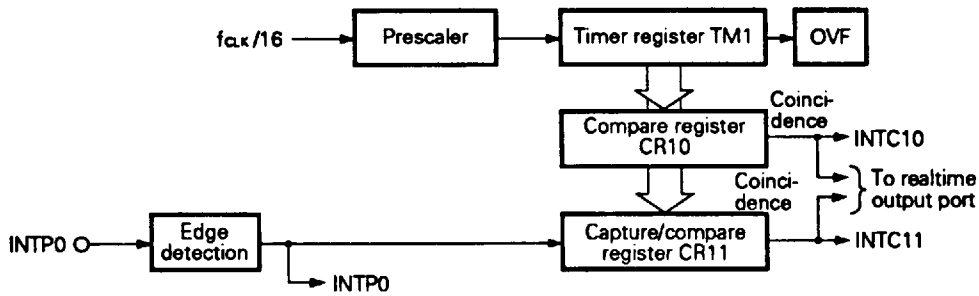
Table 2-2 Functions of Timer/Counter Unit

Type/Function \ Unit		16-Bit Timer/Counter	8-Bit Timer/Counter 1	8-Bit Timer/Counter 2
Type	Interval timer	2-ch	2-ch	2-ch
	External event counter	—	—	O
	One-shot timer	—	—	O
Function	Timer output	2-ch	—	2-ch
	Toggle output	O	—	O
	Real-time output	—	O	—
	Pulse length measurement	O	O	O
	Interrupt request	2	2	1

16-bit timer/counter unit



8-bit timer/counter unit 1



8-bit timer/counter unit 2

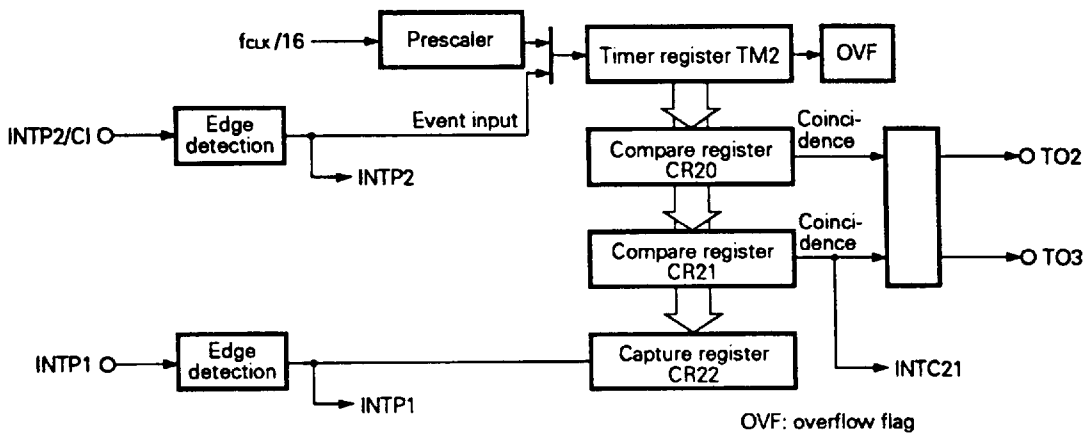


Fig. 2-5 Timer/Counter Unit Block Diagram

2.5 SERIAL INTERFACE

The μPD78220/μPD78224 incorporates the following two independent channels for serial interface functions. Therefore, external system communications and internal system communications can be performed simultaneously as shown in Fig. 2-6.

- Asynchronous serial interface
- Clock-synchronized serial interface
  3-line I/O mode (compatible conventional method)
  Serial bus interface (SBI) mode •

In addition, the μPD78220/μPD78224 has an 8-bit timer/counter for the baud rate generator so that an arbitrary baud rate can be specified.

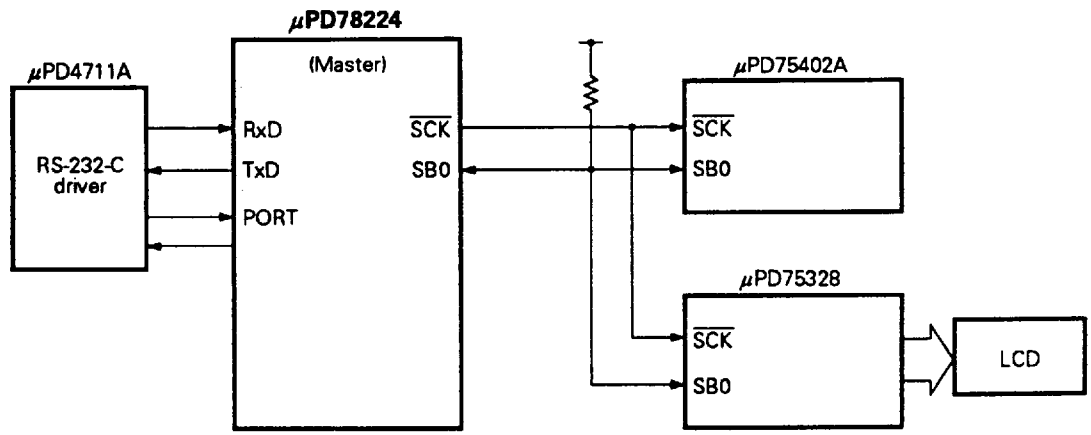


Fig. 2-6 Typical Example of Serial Interface

• : Serial bus interface (SBI)
This mode uses only 2 lines — a serial clock ($\overline{SCK}$) and serial data bus (SB0)— to communicate with multi-devices. "Addresses", "Commands", and "Data" can be sent or received by manipulating the format on the serial data bus.

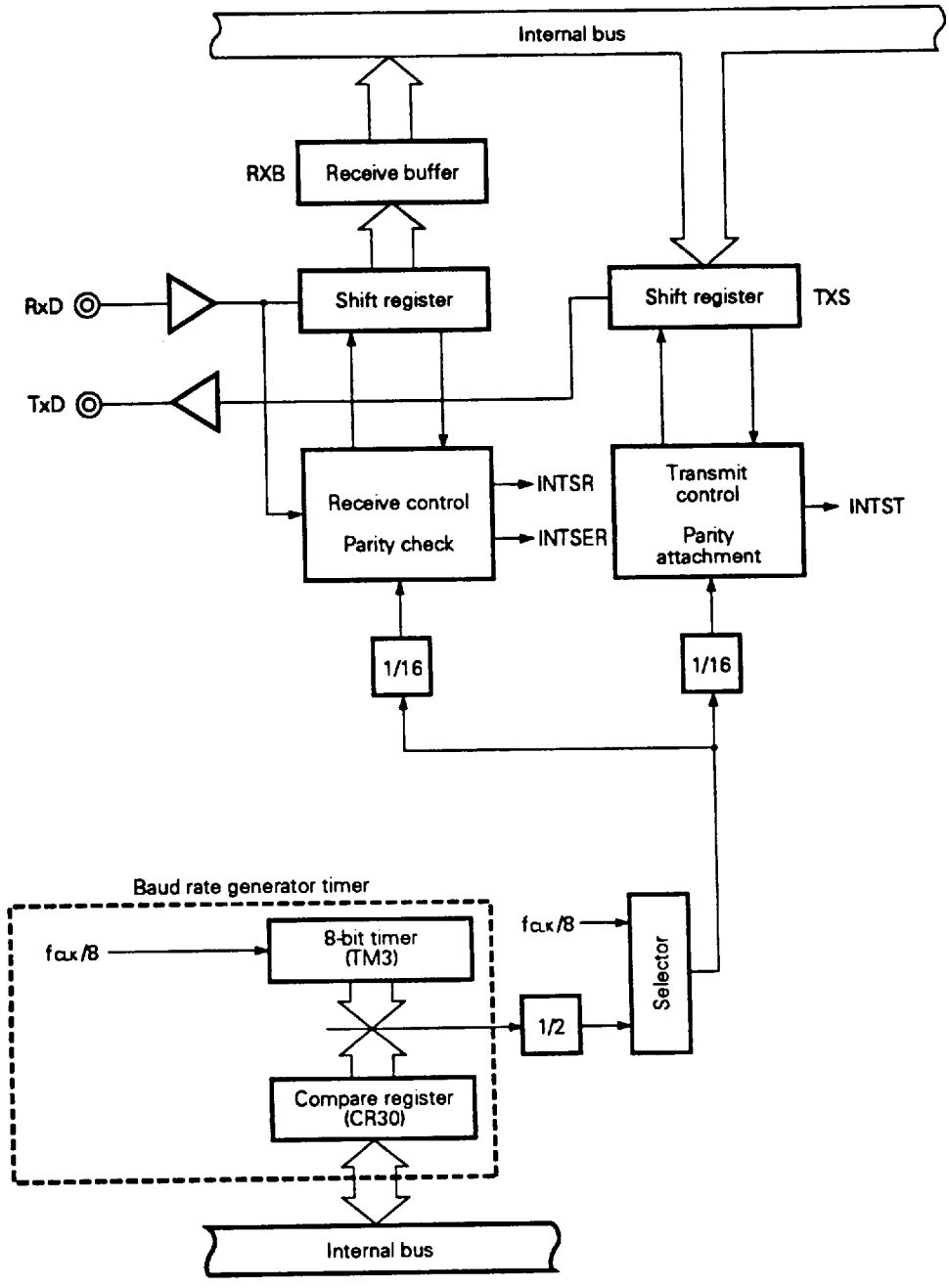


Fig. 2-7 Asynchronous Serial Interface Block Diagram

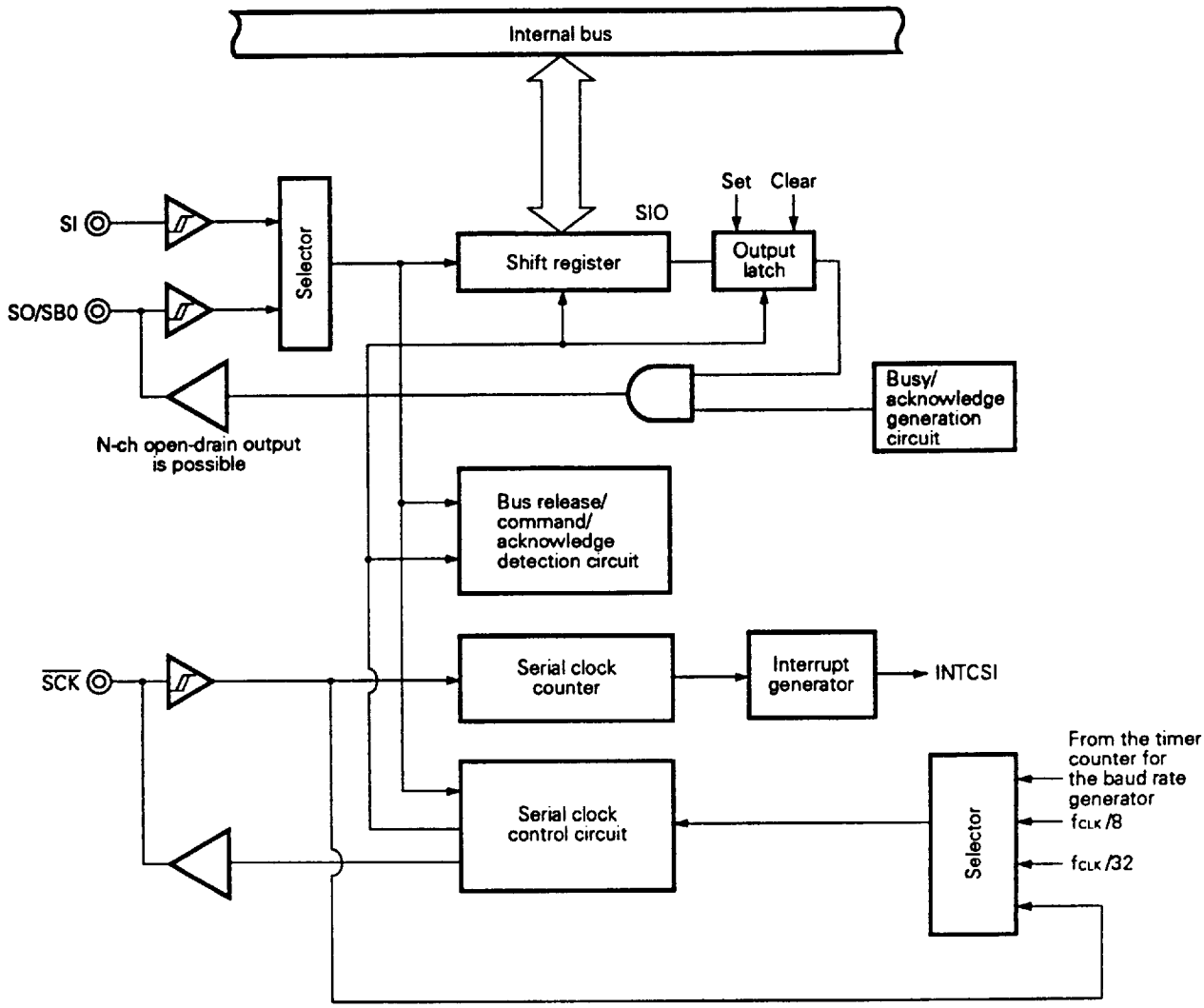


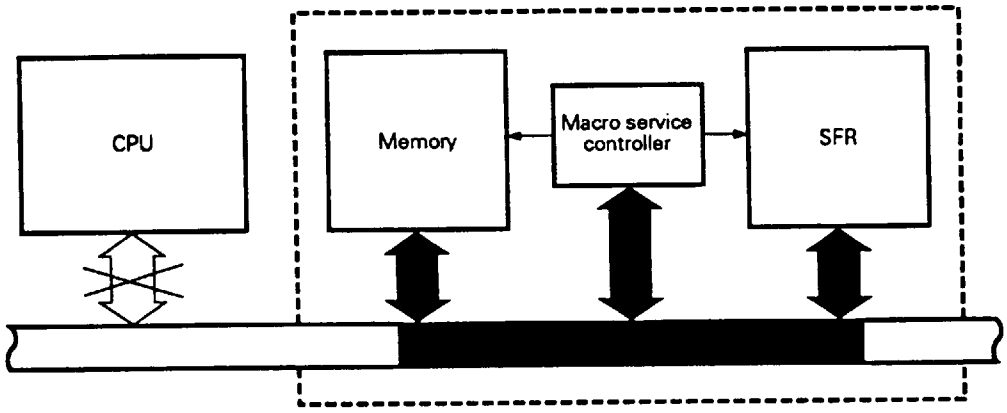
Fig. 2-8 Clock-synchronized Serial Interface Block Diagram

3. INTERRUPT FUNCTIONS

The μPD78220/μPD78224 has the following two interrupt request service modes.

- Vector interrupt (two levels of priority can be set by software)
- Macro service

In the macro service processing mode, data processing between the memory and a special function register (SFR) is directly controlled by hardware without CPU intervention.



Data transfers or arithmetic operations between an SFR and the memory are directly controller by the macro service controller.

The CPU status (SP, PSW) need not be saved/restored. Therefore, CPU overhead can be reduced.

Fig. 3-1 Macro Service Overview

3.1 INTERRUPT REQUEST SOURCES

As indicated in Table 3-1, list interrupt request sources of μPD78220/μPD78224, a vector table is provided for each interrupt request source. The macro service processing can be set to 6 interrupt request sources. The priority order of each interrupt request can be in 2 levels. Therefore, multi-interrupt control can be easily performed.

Table 3-1 Interrupt Request Sources

Type of Interrupt Request	Default Priority	Interrupt Request Source	Macro-Service Handling Mode	Vector Table Address
Software Interrupt	None	BRK instruction execution	—	003EH
Non-Maskable Interrupt	None	NMI (pin input edge detection)	—	0002H
Maskable Interrupt	0	INTP0 (pin input edge detection)	—	0006H
	1	INTP1 (pin input edge detection)	—	0008H
	2	INTP2 (pin input edge detection)	—	000AH
	3	INTP3 (pin input edge detection)	—	000CH
	4	INTC00 (TM0 - CR00 coincidence signal generation)	—	0014H
	5	INTC01 (TM0 - CR01 coincidence signal generation)	—	0016H
	6	INTC10 (TM1 - CR10 coincidence signal generation)	Provided	0018H
	7	INTC11 (TM1 - CR11 coincidence signal generation)	Provided	001AH
	8	INTC21 (TM2 - CR21 coincidence signal generation)	—	001CH
	9	INTP4 (pin input edge detection)	Provided	000EH
	10	INTP5 (pin input edge detection)	—	0010H
	11	INTP6 (pin input edge detection)	—	0012H
	12	INTSER (asynchronous serial interface receive error generation)	—	0020H
	13	INTSR (asynchronous serial interface receive completion)	Provided	0022H
	14	INTST (asynchronous serial interface transmit completion)	Provided	0024H
	15	INTCSI (clock synchronized serial interface transfer completion)	Provided	0026H

Remarks 1 : Default priority is the priority used when two or more interrupt requests are generated simultaneously.

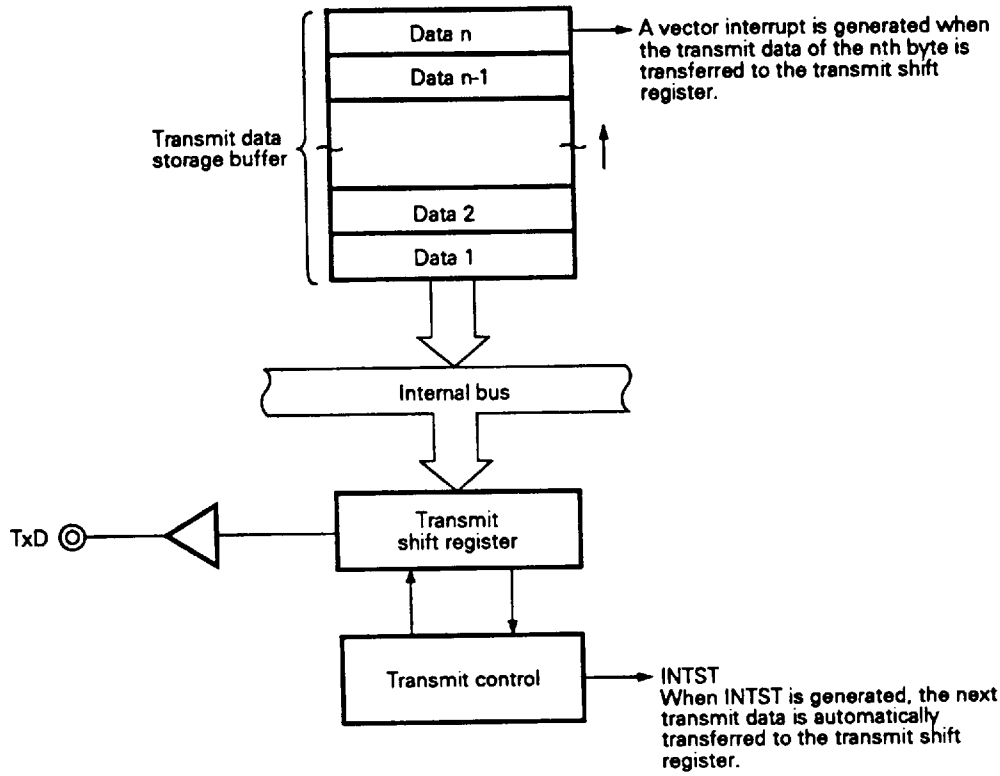
2 : Interrupt requests are divided into these three types:

- Non-maskable requests
- Maskable requests
- Software requests

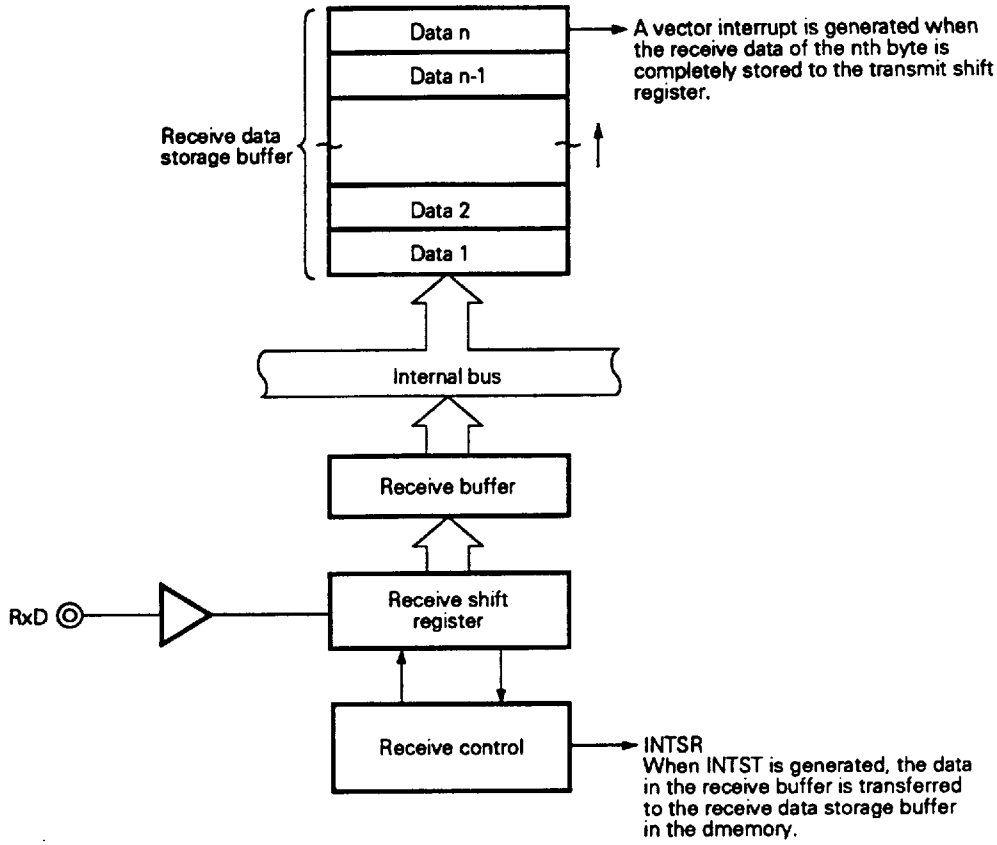
3.2 MACRO SERVICE FUNCTIONS

The following shows examples of macro service processing.

(1) Serial interface transmit operation

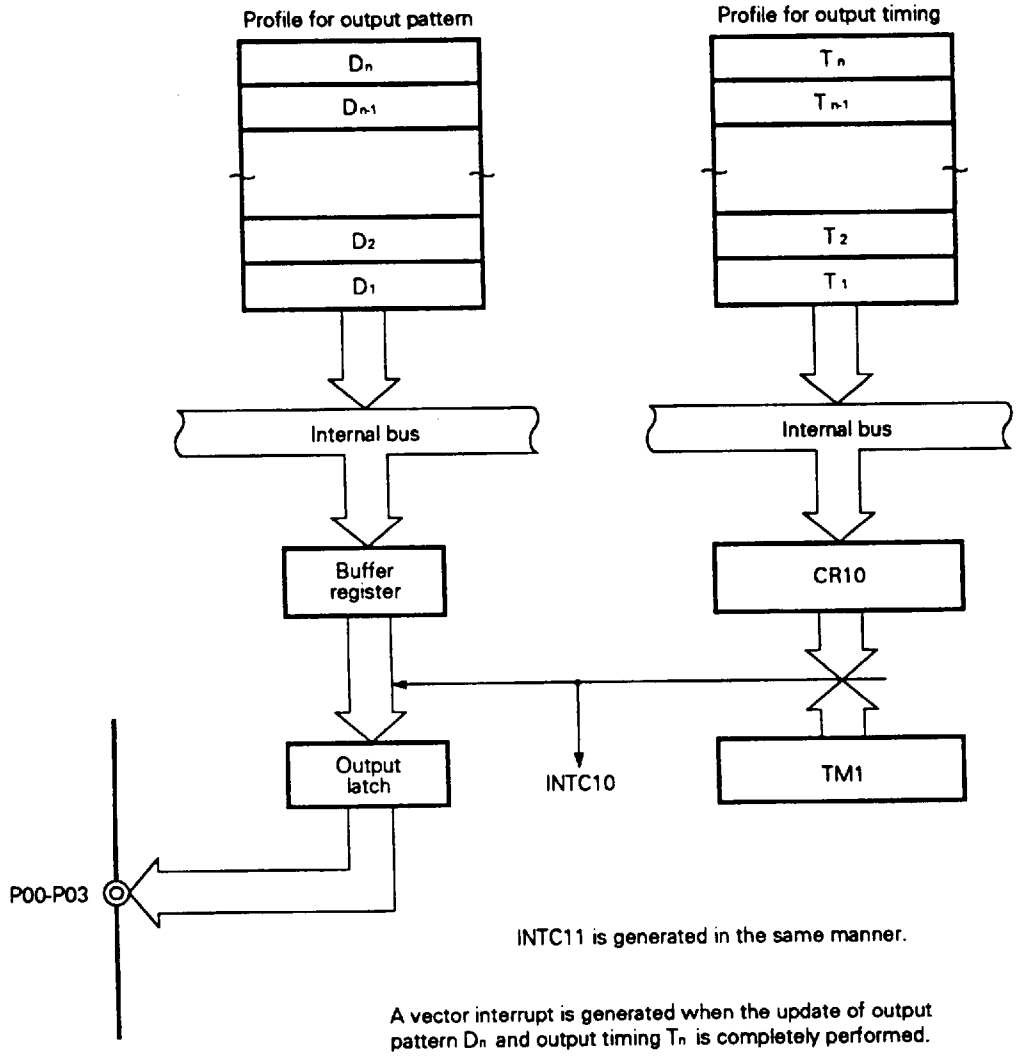


(2) Serial interface receive operation



(3) Real-time output port control

For macro service which uses INTC10 and INTC11 as the output triggers for the real-time output port, the next output pattern and the next output interval data can be set in one macro service processing. With this function, a two-channel stepping motor system can be independently controlled. In addition, this function can be used for various applications such as PWM output or DC motor control.



INTC11 is generated in the same manner.

A vector interrupt is generated when the update of output pattern D_n and output timing T_n is completely performed.

4. LOCAL BUS INTERFACE FUNCTIONS

The μPD78224 has an internal 16K-byte ROM. However, the external memory and I/O can be expanded up to 48K bytes using the external memory expansion function. If the $\overline{EA}$ pin is set to low, the μPD78224 operates in the ROM-less mode. In this case, the internal ROM is not used, and up to 64K bytes of external memory and I/O can be connected.

The μPD78220 has no internal ROM. Therefore, it requires both an external ROM and I/O (up to 64K bytes).

For the μPD78220/μPD78224, the data memory can be expanded up to 1M byte (1M-byte expansion function). In this case, pins P60 to P63 serve as the upper 4 bits of the address bus (A16-A19).

< Major features >

The following functions are supported.

1. Data memory space can be expanded up to 1M byte.
2. Programmable wait function
   Wait cycles can be inserted independently into the memory-mapped 64K-byte space (00000H to 0FFFFH) and the 1M-byte expansion space (10000H to FFFFFH). Therefore, a significant reduction in overall system processing speed can be prevented when a slow-speed memory is connected.
3. Supports pseudo-static RAM refresh function.
   - Pulse refresh function
   - Self refresh function

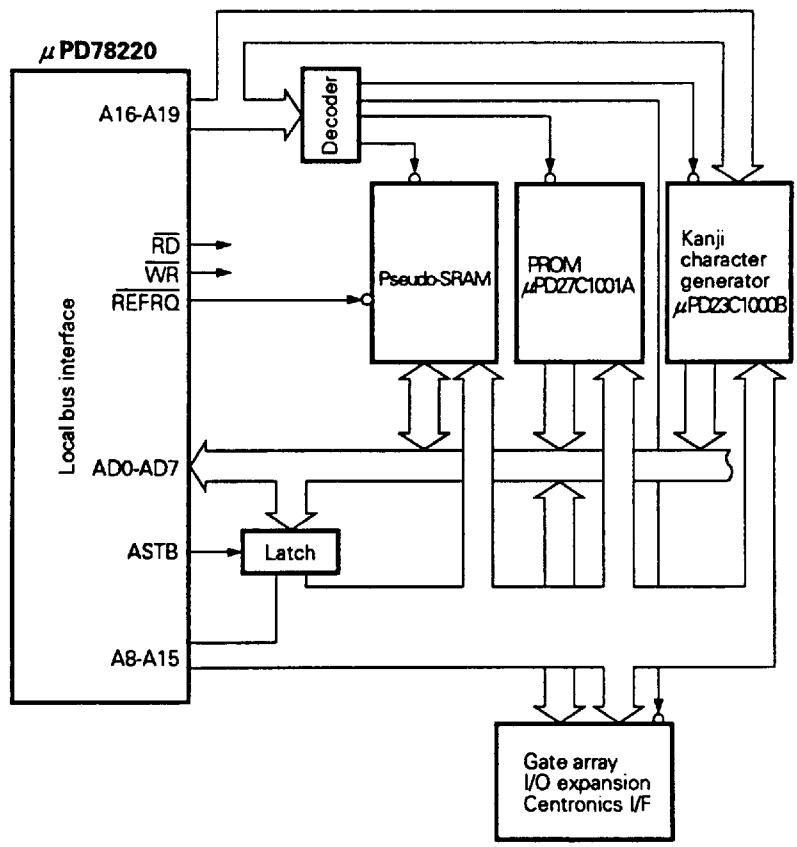


Fig. 4-1 Typical Example of Local Bus Interface

5. STANDBY FUNCTIONS

In the μPD78220/μPD78224, the following two standby modes are provided in order to reduce overall system power consumption.

- HALT mode ------ In this mode, the CPU operation clock is stopped. When combined with the normal mode, the total power consumption of the system can be reduced by intermittent operation.
- STOP mode ------ In this mode, the clock oscillator is stopped so that the entire system operation is stopped. In this mode, the operating current is reduced to the leakage current level.

Each mode is set by means of software. Fig. 5-1 shows the standby mode (STOP/HALT) transition diagram.

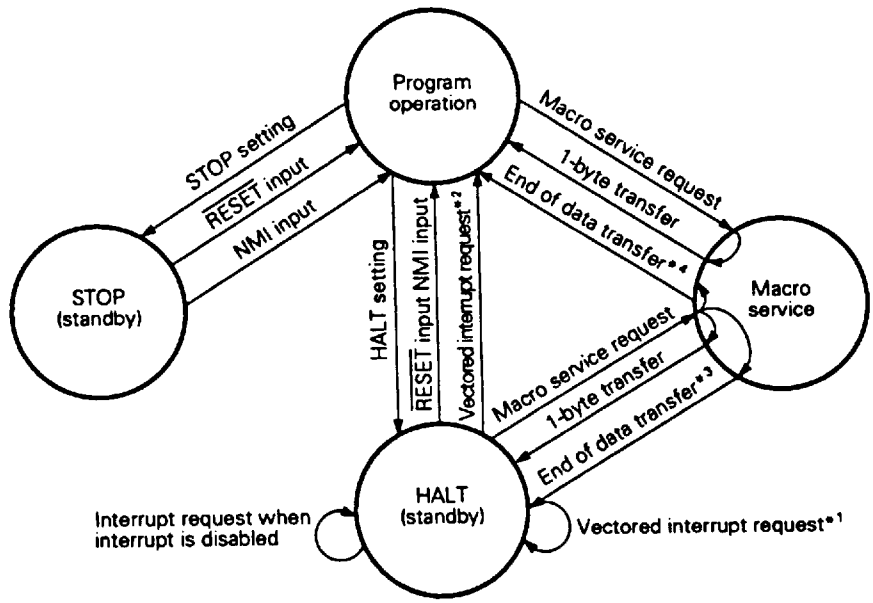


Fig. 5-1 Transition to/from Standby Modes

*1: In the case of a vectored interrupt with a low priority (The low-priority interrupt is disabled in the HALT mode.)

*2: In the case of a vectored interrupt with a high priority, or when the interrupt with a low priority is enabled in the HALT mode.

*3: In the case of macro service with a low priority (when the interrupt with a low priority is disabled in the HALT mode)

*4: In the case of macro service with a high priority, or when the interrupt with a low priority is enabled in the HALT mode

6. RESET FUNCTIONS

When a low level is input to the $\overline{\text{RESET}}$ input pin, a system reset is effected, and each piece of hardware enters the state indicated in Table 6-1.

When the $\overline{\text{RESET}}$ input changes from low to high, the reset state is released, and the contents of address 00000H of the reset vector table are loaded to bits 7 to 0 in the program counter (PC); the contents of address 00001H in the reset vector table are loaded to bits 15 to 8 of the program counter (PC), and branching is performed. Program execution then starts from the branch destination address. Therefore, a reset start can be executed from an arbitrary address.

The contents of each register must be initialized in the program as necessary.

In order to prevent erroneous operation, the $\overline{\text{RESET}}$ input pin has an analog delay noise elimination circuit (refer to Figure 6-1). As shown in Figure 6-2, an oscillation stabilization time of approximately 40ms should be assured before releasing the reset from the time of power application.

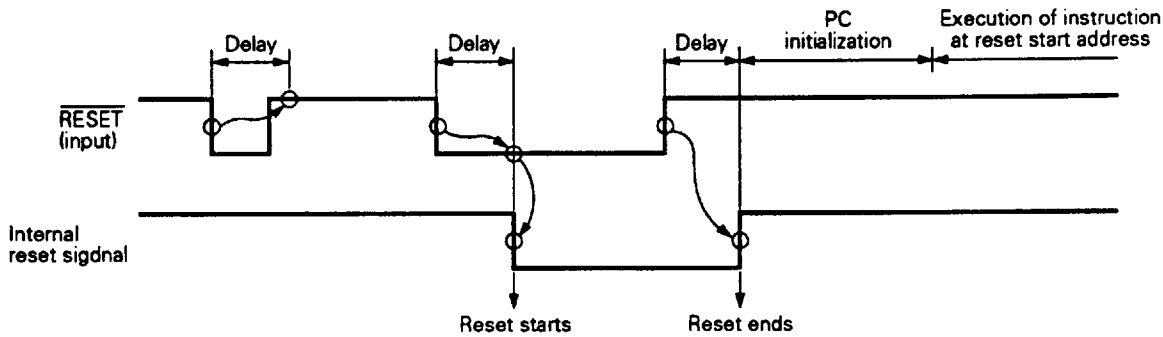


Fig. 6-1 Acceptance of $\overline{\text{RESET}}$ Signal

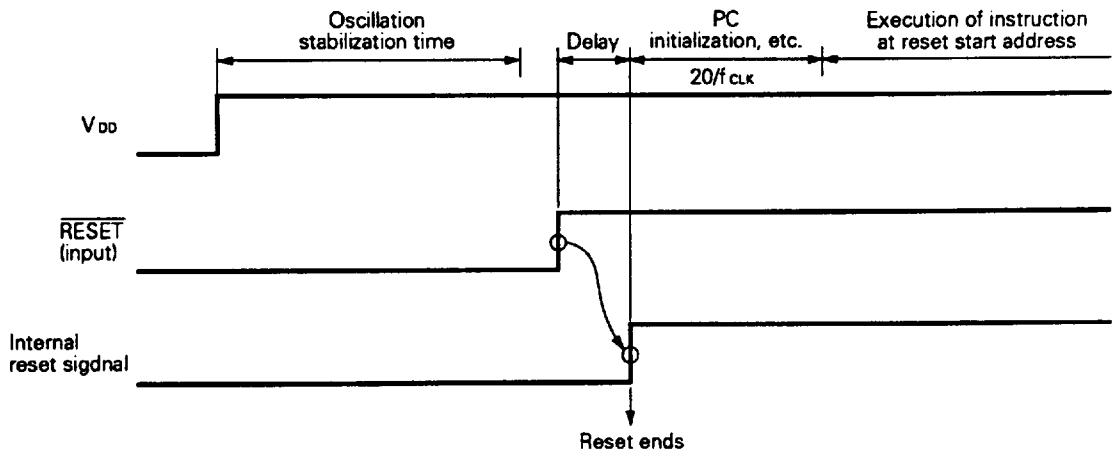


Fig. 6-2 Reset Upon Power Application

Remarks: f_{CLK}: system clock frequency (fxx/2)

Table 6-1 Hardware Status after Reset

Hardware			Status After Reset
Program counter (PC)			The contents of the reset vector table (00000H, 00001H) are loaded
Stack pointer (SP)			Undefined*
Program status word (PSW)			02H
Internal RAM	Data memory		Undefined*
	General purpose registers (X, A, C, B, E, D, L, H)		
Port	Ports 0, 1, 2, 3, 4, 5, 7, and T		Undefined (high impedance)
	Port 6		X0H
	Port mode register	PM0, PM1, PM3, PM5	FFH
		PM6	FXH
		PM7	7FH
		PMT	00H
	Port 3 mode control register (PMC3)		00H
Real-time output port control register (RTPC)			00H
Memory expansion mode register (MM)			20H
Timer/counter unit	16-bit timer/counter	Timer (TM0)	0000H
		Compare registers (CR00, CR01)	Undefined
		Capture register (CR02)	
	8-bit timer/counter	8-bit timers (TM1, TM2, TM3)	00H
		Compare registers (CR10, CR20, CR21, CR30)	Undefined
		Capture register (CR22)	
		Capture/compare register (CR11)	
	Timer control registers (TMC0, TMC1)		00H
	Timer output control register (TOC)		
	Capture/compare register control register (CRC0)		10H
	Capture/compare register control registers (CRC1, CRC2)		00H
	Pre-scaler mode registers (PRM0, PRM1)		00H
Serial interface	Mode register (CSIM)		00H
	Shift register (SIO)		Undefined
	Asynchronous mode register (ASIM)		80H
	Asynchronous status register (ASIS)		00H
	Serial bus control register (SBIC)		00H
	Serial receive buffer (RXB)		Undefined
	Serial transmit shift register (TXS)		Undefined
Programmable wait control register (PW)			80H
Refresh mode register (RFM)			00H
Interrupt	Interrupt request flag register (IF0)		0000H
	Interrupt mask register (MK0)		FFFFH
	Interrupt priority specification flag register (PR0)		FFFFH
	Interrupt service mode register (ISM0)		0000H
	Interrupt status register (IST)		00H
External interrupt mode registers (INTM0, INTM1)			00H
Standby control register (STBC)			0000 × 000B

*: When the STOP mode is released by inputting a $\overline{\text{RESET}}$, the value of pre-STOP mode status is retained.

★ 7. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP

Table 7-1 8-Bit Instruction for Addressing

First Operand \ Second Operand	#byte	A	r r'	saddr saddr'	sfr	mem	&mem	!addr16	&!addr16	PSW	n	None*
A	ADD*1		MOV XCH	MOV XCH ADD*1	MOV XCH ADD*1	MOV XCH ADD*1	MOV XCH ADD*1	MOV	MOV	MOV		
r	MOV		MOV XCH ADD*1								ROL ROLC ROR RORC SHR SHL	MULU DIVUW INC DEC
rl												DBNZ
saddr	MOV ADD*1	MOV		MOV XCH ADD*1								INC DBNZ DEC
sfr	MOV ADD*1	MOV										PUSH POP
mem &mem		MOV										
meml &meml												ROR4 ROL4
!addr16		MOV										
&!addr16		MOV										
PSW	MOV	MOV										PUSH POP
STBC	MOV											

*1: ADD can be replaced by ADDC, SUB, SUBC, AND, OR, XOR, or CMP.

2: Second operand is not needed or is not operand address.

(2) 16-bit instruction

MOVW, ADDW, SUBW, CMPW, INCW, DECW, SHRW, SHLW, PUSH, POP

Table 7-2 16-Bit Instruction for Addressing

First Operand \ Second Operand	#word	AX	rp rp'	saddrp	sfrp	meml	&meml	SP	n	None
AX	ADDW SUBW CMPW		ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW	MOVW	MOVW		
rp	MOVW		MOVW						SHLW SHRW	INCW DECW PUSH POP
saddrp	MOVW	MOVW								
sfrp	MOVW	MOVW								
meml &meml		MOVW								
SP	MOVW	MOVW								INCW DECW

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Table 7-3 Bit Manipulation Instruction for Addressing

First Operand \ Second Operand	CY	A.bit	/A.bit	X.bit	/X.bit	saddr. bit	/saddr. bit	sfr.bit	/sfr.bit	PSW.bit	/PSW. bit	None*
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	SET1 CLR1 NOT1
A.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
X.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
saddr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
sfr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
PSW.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR

*: Second operand is not needed or is not operand address.

(4) Call/branch instructions

CALL, CALLF, CALLT, BR, BC, BT, BF, BTCLR, DBNZ, BL, BNC, BNL, BZ, BE, BNZ, BNE

Table 7-4 Call/Branch Instructions for Addressing

Operand of Instruction Address	$addr16	!addr16	rp	!addr11	[addr5]
Basic Operation	BR BC*	CALL BR	CALL BR	CALLF	CALLT
Compound Operation	BT BF BTCLR DBNZ				

*: BC can be replaced by BL, BNC, BNL, BZ, BE, BNZ, or BNE.

(5) Other Instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, NOP, EI, DI, SEL

8. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	Symbol	Conditions	Ratings	Unit
Operating Voltage	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_I		−0.5 to V_{DD} +0.5	V
Output Voltage	V_O		−0.5 to V_{DD} +0.5	V
Low-Level Output Current	I_{OL}	1 pin	30 (Peak)	mA
			15 (Mean value)	mA
		All output pins total	150 (Peak)	mA
			100 (Mean value)	mA
High-Level Output Current	I_{OH}	1 pin	−2	mA
		All output pins total	−50	mA
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

★ **Note:** Even if one of the parameters exceed its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.

OPERATING CONDITIONS

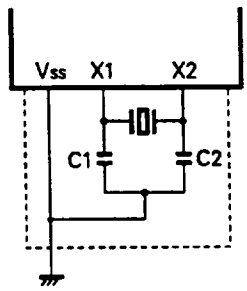
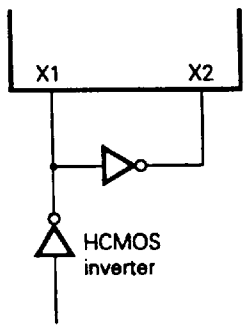
Parameter / Oscillation Frequency	T_a	V_{DD}
4MHz ≤ f_{XX} ≤ 12MHz	-10 to +70 °C	+5 V ±10 %
4MHz ≤ f_{XX} ≤ 12MHz	-40 to +85 °C	+5 V ±5 %

CAPACITANCE (T_a = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_I	f = 1 MHz			20	pF
Output Capacitance	C_O	Pins not used for measurement are at 0 V			20	pF
Input/Output Capacitance	C_{IO}				20	pF

(1) T_a = −10 to +70 °C

OSCILLATOR CHARACTERISTICS (T_a = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Resonator	Recommended Circuit	Item	MIN.	MAX.	Unit
Ceramic or Crystal Resonator		Oscillation frequency (f_{XX})	4	12	MHz
External Clock		X1 input frequency (f_X)	4	12	MHz
		X1 input rise/fall time (t_{XR}, t_{XF})	0	30	ns
		X1 input high-/low-level range (t_{WXH}, t_{WXL})	30	130	ns

Note: When using the oscillation circuit of the clock wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines.
- Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as Vss. Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuits.

RECOMMENDED OSCILLATION CIRCUIT CONSTANT

Crystal resonator

Manufacturer	Frequency [MHz]	Product	Recommended Constant	
			C1 [pF]	C2 [pF]
Kinseki	10	HC-18/U, 43/U, 49/U	27	22

Ceramic resonator

Manufacturer	Product	Recommended Constant	
		C1 [pF]	C2 [pF]
Murata	CSA10.0MT040	100	100
	CSA12.0MT040	100	100
Kyocera	KBR-10.0M	33	33

DC CHARACTERISTICS (T_a = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-Level Input Voltage	V_{IL}	Except the PT pin		0		0.8	V
High-Level Input Voltage	V_{IH1}	Except the PT pin and the specified pins*		2.2		V_{DD}	V
	V_{IH2}	Specified pins*		0.8 V_{DD}		V_{DD}	V
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2.0 mA				0.45	V
	V_{OL2}	I_{OL} = 8.0 mA (Port 1 pin)				1.0	V
High-Level Output Voltage	V_{OH1}	I_{OH} = −1.0 mA		V_{DD} − 1.0			V
	V_{OH2}	I_{OH} = −100 μA		V_{DD} − 0.5			V
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0V ≤ V_O ≤ V_{DD}				±10	μA
Pull-Up Current	I_{IPT}	V_I(PT pin) = 0 V			−150	−400	μA
V_{DD} Power Supply Current	I_{DD1}	Operating mode, f_{XX} = 12 MHz			16	40	mA
	I_{DD2}	HALT mode, f_{XX} = 12 MHz			7	20	mA
Data Retention Voltage	V_{DDDR}	STOP mode		2.5		5.5	V
Data Retention Current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	20	μA
			V_{DDDR} = 5 V ±10 %		5	50	μA

* : X1, X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, and $\overline{\text{EA}}$ pins.

AC CHARACTERISTICS (T_a = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

READ/WRITE OPERATION

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	
X1 Input Clock Cycle Time	t_{CYX}		82	250	ns	
Address Set-Up Time (Against ASTB ↓)	t_{SAST} *		52		ns	
Address Hold Time (Against ASTB ↓)	t_{HSTA}	R_L = 5 kΩ, C_L = 50 pF	25		ns	
Address → $\overline{RD}$ ↓ Delay Time	t_{DAR} *		129		ns	
Address Float Time (Against $\overline{RD}$ ↓)	t_{FAR} *		11		ns	
Address → Data Input Time	t_{DAID} *	w/o wait		228	ns	
ASTB ↓ → Data Input Time	t_{DSTID} *	w/o wait		181	ns	
$\overline{RD}$ ↓ → Data Input Time	t_{DRID} *	w/o wait		100	ns	
ASTB ↓ → $\overline{RD}$ ↓ Delay Time	t_{DSTR} *		52		ns	
Data Hold Time (Against $\overline{RD}$ ↑)	t_{HRID}		0		ns	
$\overline{RD}$ ↑ → Address Active Time	t_{DRA} *		124		ns	
$\overline{RD}$ ↑ → ASTB ↑ Delay Time	t_{DRST} *		124		ns	
$\overline{RD}$ Low-Level Range	t_{WRL} *	w/o wait	124		ns	
ASTB High-Level Range	t_{WSTH} *		52		ns	
Address → $\overline{WR}$ ↓ Delay Time	t_{DAW} *		129		ns	
ASTB ↓ → Data Output Time	t_{DSTOD} *			142	ns	
$\overline{WR}$ ↓ → Data Output Time	t_{DWOD}			60	ns	
ASTB ↓ → $\overline{WR}$ ↓ Delay Time	t_{DSTW1} *	Refresh disabled	52		ns	★
	t_{DSTW2} *	Refresh enabled	129		ns	
Data Set-Up Time (Against $\overline{WR}$ ↑)	t_{SODWR} *	w/o wait	146		ns	
Data Set-Up Time (Against $\overline{WR}$ ↓) Note 1	t_{SODWF} *	Refresh enabled	22		ns	
Data Hold Time (Against $\overline{WR}$ ↑) Note 2	t_{HWOD}		20		ns	
$\overline{WR}$ ↑ → ASTB ↑ Delay Time	t_{DWST} *		42		ns	
$\overline{WR}$ Low-Level Range	t_{WWL1} *	Refresh disabled w/o wait	196		ns	★
	t_{WWL2} *	Refresh enabled w/o wait	114		ns	
Address → $\overline{WAIT}$ ↓ Input Time	t_{DAWT} *			146	ns	
ASTB ↓ → $\overline{WAIT}$ ↓ Input Time	t_{DSTWT} *			84	ns	
$\overline{WAIT}$ Hold Time (Against X1 ↓)	t_{HWTX}		0		ns	
$\overline{WAIT}$ Set-Up Time (Against X1 ↑)	t_{SWTX}		0		ns	

Note 1 : When accessing a pseudo-static RAM (μPD4168, etc.) which clocks in data at the falling edge of the $\overline{WR}$ signal, use t_{SODWF} instead of t_{SODWR} as the data set up time.

2 : The hold time includes the time during which V_{OH} and V_{OL} are retained under the following load conditions; C_L = 100 pF and R_L = 2 kΩ.

Remarks 1 : Values in this table are at f_{XX} = 12 MHz, C_L = 100 pF.

2 : For * mark, refer to DEFINITION OF BUS TIMING DEPENDING ON t_{CYX}.

SERIAL OPERATION

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial Clock Cycle Time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internal clock/16	1.3		μs
			Internal clock/64	5.3		μs
Serial Clock Low-Level Range	t_{WSKL}	Input	External clock	420		ns
		Output	Internal clock/16	556		ns
			Internal clock/64	2.5		μs
Serial Clock High-Level Range	t_{WSKH}	Input	External clock	420		ns
		Output	Internal clock/16	556		ns
			Internal clock/64	2.5		μs
SI, SB0 Set-Up Time (Against $\overline{SCK}$ ↑)	t_{SSSK}			150		ns
SI, SB0 Hold Time (Against $\overline{SCK}$ ↑)	t_{HSSK}			400		ns
SO/SB0 Output Delay Time (Against $\overline{SCK}$ ↓)	t_{DSSSK1}	CMOS push-pull output (3-line serial I/O mode)		0	300	ns
	t_{DSSSK2}	Open-drain output (SBI mode), R_L = 1 KΩ		0	800	ns
SB0 High Hold Time (Against $\overline{SCK}$ ↑)	t_{HSSSK}	SBI mode		4		t_{CYX}
SB0 Low Set-Up Time (Against $\overline{SCK}$ ↓)	t_{SSSSK}			4		t_{CYX}
SB0 Low-Level Range	t_{WSSL}			4		t_{CYX}
SB0 High-Level Range	t_{WSSH}			4		t_{CYX}

Remarks : Values in the table are for f_{XX} = 12 MHz, C_L = 100 pF.

OTHER OPERATION

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI Low-Level Range	t_{WNIL}		10		μs
NMI High-Level Range	t_{WNIH}		10		μs
INTP0-INTP6 Low-Level Range	t_{WITL}		24		t_{CYX}
INTP0-INTP6 High-Level Range	t_{WITH}		24		t_{CYX}
$\overline{\text{RESET}}$ Low-Level Range	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ High-Level Range	t_{WRSH}		10		μs

EXTERNAL CLOCK TIMING

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
X1 Input Low-Level Range	t_{WXL}		30	130	ns
X1 Input High-Level Range	t_{WXH}		30	130	ns
X1 Input Rise Time	t_{XR}		0	30	ns
X1 Input Fall Time	t_{XF}		0	30	ns
X1 Input Clock Cycle Time	t_{CYX}		82	250	ns

COMPARATOR CHARACTERISTICS (Ta = −10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Comparison Accuracy	V_{ACOMP}				100	mV
Comparison Time	t_{COMP}		128		256	t_{CYX}
Sampling Time	t_{SAMP}		62			t_{CYX}
PT Input Voltage	V_{IPT}		0		V_{DD}	V

DEFINITION OF BUS TIMING DEPENDING ON t_{CYX}

	Parameter	Symbol	Calculation Formula	MIN./MAX.	12 MHz	Unit
	X1 Input Clock Cycle Time	t_{CYX}		MIN.	82	ns
	Address Set-Up Time (Against ASTB ↓)	t_{SAST}	$t_{CYX} - 30$	MIN.	52	ns
	Address → $\overline{RD}$ ↓ Delay Time	t_{DAR}	$2t_{CYX} - 35$	MIN.	129	ns
	Address Float Time (Against $\overline{RD}$ ↓)	t_{FAR}	$t_{CYX}/2 - 30$	MIN.	11	ns
	Address → Data Input Time	t_{DAID}	$(4 + 2n)\ t_{CYX} - 100$	MAX.	228*	ns
	ASTB ↓ → Data Input Time	t_{DSTID}	$(3 + 2n)\ t_{CYX} - 65$	MAX.	181*	ns
	$\overline{RD}$ ↓ → Data Input Time	t_{DRID}	$(2 + 2n)\ t_{CYX} - 64$	MAX.	100*	ns
	ASTB ↓ → $\overline{RD}$ ↓ Delay Time	t_{DSTR}	$t_{CYX} - 30$	MIN.	52	ns
	$\overline{RD}$ ↑ → Address Active Time	t_{DRA}	$2t_{CYX} - 40$	MIN.	124	ns
	$\overline{RD}$ ↑ → ASTB ↑ Delay Time	t_{DRST}	$2t_{CYX} - 40$	MIN.	124	ns
	$\overline{RD}$ Low-Level Range	t_{WRL}	$(2 + 2n)\ t_{CYX} - 40$	MIN.	124*	ns
	ASTB High-Level Range	t_{WSTH}	$t_{CYX} - 30$	MIN.	52	ns
	Address → $\overline{WR}$ ↓ Delay Time	t_{DAW}	$2t_{CYX} - 35$	MIN.	129	ns
	ASTB ↓ → Data Output Time	t_{DSTOD}	$t_{CYX} + 60$	MAX.	142	ns
★	ASTB ↓ → $\overline{WR}$ ↓ Delay Time	t_{DSTW1}	$t_{CYX} - 30$ (Refresh disabled)	MIN.	52	ns
		t_{DSTW2}	$2t_{CYX} - 35$ (Refresh enabled)	MIN.	129	ns
	Data Set-Up Time (Against $\overline{WR}$ ↑)	t_{SODWR}	$(3 + 2n)\ t_{CYX} - 100$	MIN.	146*	ns
	Data Set-Up Time (Against $\overline{WR}$ ↓)	t_{SODWF}	$t_{CYX} - 60$ (Refresh enabled)	MIN.	22	ns
	$\overline{WR}$ ↑ → ASTB ↑ Delay Time	t_{DWST}	$t_{CYX} - 40$	MIN.	42	ns
★	$\overline{WR}$ Low-Level Range	t_{WWL1}	$(3 + 2n)\ t_{CYX} - 50$ (Refresh disabled)	MIN.	196*	ns
		t_{WWL2}	$(2 + 2n)\ t_{CYX} - 50$ (Refresh enabled)	MIN.	114*	ns
	Address → $\overline{WAIT}$ ↓ Input Time	t_{DAWT}	$3t_{CYX} - 100$	MAX.	146	ns
	ASTB ↓ → $\overline{WAIT}$ ↓ Input Time	t_{DSTWT}	$2t_{CYX} - 80$	MAX.	84	ns

*: When n = 0

Remarks : n indicates the number of WAIT states.

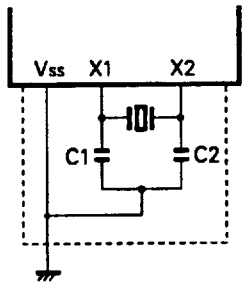
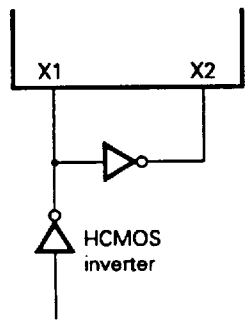
DATA RETENTION CHARACTERISTICS (Ta = –10 to +70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data Retention Current	I_{DDDR}	V_{DDDR} = 2.5 V		2	20	μA
		V_{DDDR} = 5 V ± 10 %		5	50	μA
V_{DD} Rise Time	t_{RVD}		200			μs
V_{DD} Fall Time	t_{FVD}		200			μs
V_{DD} Retention Time (for STOP Mode Setting)	t_{HVD}		0			ms
STOP Selease Signal Input Time	t_{DREL}		0			ms
Oscillation Stabilization Wait Time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-Level Input Voltage	V_{IL}	Specified pins*	0		0.1 V_{DDDR}	V
High-Level Input Voltage	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

* : $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, and $\overline{\text{EA}}$ pins.

(2) T_a = –40 to +85 °C

OSCILLATOR CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = +5 V ±5 %, Vss = 0 V)

Resonator	Recommended Circuit	Item	MIN.	MAX.	Unit
Ceramic or Crystal Resonator		Oscillation frequency (f_{XX})	4	12	MHz
External Clock		X1 input frequency (f_X)	4	12	MHz
		X1 input rise/fall time (t_{XR}, t_{XF})	0	30	ns
		X1 input high-/low-level range (t_{WXH}, t_{WXL})	30	130	ns

Note: When using the oscillation circuit of the clock wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines.
- Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as Vss. Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuits.

RECOMMENDED OSCILLATION CIRCUIT CONSTANT

Crystal resonator

Manufacturer	Frequency [MHz]	Product	Recommended constant	
			C1 [pF]	C2 [pF]
Kinseki	10	HC-18/U, 43/U, 49/U*1	27	22

Ceramic resonatory

Manufacturer	Product	Recommended constant	
		C1 [pF]	C2 [pF]
Murata	CSA10.0MT040	100	100
	CSA12.0MT040*2	100	100
Kyocera	KBR-10.0M	33	33

*1 : When using this resonator operating temperature range should be –20 to +70 °C.

*2 : When using this resonator operating temperature range should be –20 to +85 °C.

DC CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = +5 V ±5 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-Level Input Voltage	V_{IL}	Except the PT pin		0		0.8	V
High-Level Input Voltage	V_{IH1}	Except the PT pin and the specified pins*		2.2		V_{DD}	V
	V_{IH2}	Specified pins*		0.8 V_{DD}		V_{DD}	V
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2.0 mA				0.45	V
	V_{OL2}	I_{OL} = 8.0 mA (Port 1 pin)				1.0	V
High-Level Output Voltage	V_{OH1}	I_{OH} = –1.0 mA		V_{DD} – 1.0			V
	V_{OH2}	I_{OH} = –100 μA		V_{DD} – 0.5			V
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0V ≤ V_O ≤ V_{DD}				±10	μA
Pull-Up Current	I_{IPT}	V_I(PT pin) = 0 V			–150	–400	μA
V_{DD} Power Supply Current	I_{DD1}	Operating mode, f_{XX} = 12 MHz			16	40	mA
	I_{DD2}	HALT mode, f_{XX} = 12 MHz			7	20	mA
Data Retention Voltage	V_{DDDR}	STOP mode		2.5		5.5	V
Data Retention Current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	20	μA
			V_{DDDR} = 5 V ±10 %		5	50	μA

* : X1, X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, and $\overline{\text{EA}}$ pins.

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +5 V ±5 %, V_{SS} = 0 V)

READ/WRITE OPERATION

	Parameter	Symbol	Conditions	MIN.	MAX.	Unit
	X1 Input Clock Cycle Time	t_{CYX}		82	250	ns
	Address Set-Up Time (Against ASTB ↓)	t_{SAST} *		52		ns
	Address Hold Time (Against ASTB ↓)	t_{HSTA}	R_L = 5 kΩ, C_L = 50 pF	25		ns
	Address → $\overline{RD}$ ↓ Delay Time	t_{DAR} *		129		ns
	Address Float Time (Against $\overline{RD}$ ↓)	t_{FAR} *		11		ns
	Address → Data Input Time	t_{DAID} *	w/o wait		228	ns
	ASTB ↓ → Data Input Time	t_{DSTID} *	w/o wait		181	ns
	$\overline{RD}$ ↓ → Data Input Time	t_{DRID} *	w/o wait		100	ns
	ASTB ↓ → $\overline{RD}$ ↓ Delay Time	t_{DSTR} *		52		ns
	Data Hold Time (Against $\overline{RD}$ ↑)	t_{HRID}		0		ns
	$\overline{RD}$ ↑ → Address Active Time	t_{DRA} *		124		ns
	$\overline{RD}$ ↑ → ASTB ↑ Delay Time	t_{DRST} *		124		ns
	$\overline{RD}$ Low-Level Range	t_{WRL} *	w/o wait	124		ns
	ASTB High-Level Range	t_{WSTH} *		52		ns
	Address → $\overline{WR}$ ↓ Delay Time	t_{DAW} *		129		ns
	ASTB ↓ → Data Output Time	t_{DSTOD} *			142	ns
	$\overline{WR}$ ↓ → Data Output Time	t_{DWOD}			60	ns
★	ASTB ↓ → $\overline{WR}$ ↓ Delay Time	t_{DSTW1} *	Refresh disabled	52		ns
		t_{DSTW2} *	Refresh enabled	129		ns
	Data Set-Up Time (Against $\overline{WR}$ ↑)	t_{SODWR} *	w/o wait	146		ns
	Data Set-Up Time (Against $\overline{WR}$ ↓)	t_{SODWF} *	Refresh enabled	22		ns
	Data Hold Time (Against $\overline{WR}$ ↑) Note	t_{HWOD}		20		ns
	$\overline{WR}$ ↑ → ASTB ↑ Delay Time	t_{DWST} *		42		ns
★	$\overline{WR}$ Low-Level Range	t_{WWL1} *	Refresh disabled w/o wait	196		ns
		t_{WWL2} *	Refresh enabled w/o wait	114		ns
	Address → $\overline{WAIT}$ ↓ Input Time	t_{DAWT} *			146	ns
	ASTB ↓ → $\overline{WAIT}$ ↓ Input Time	t_{DSTWT} *			84	ns
	$\overline{WAIT}$ Hold Time (Against X1 ↓)	t_{HWTX}		0		ns
	$\overline{WAIT}$ Set-Up Time (Against X1 ↑)	t_{SWTX}		0		ns

Note : The hold time includes the time during which V_{OH} and V_{OL} are retained under the following load conditions; C_L = 100 pF and R_L = 2 kΩ.

Remarks 1 : Values in this table are at f_{XX} = 12 MHz, C_L = 100 pF.

2 : For * mark, refer to DEFINITION OF BUS TIMING DEPENDING ON t_{CYX}.

SERIAL OPERATION

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial Clock Cycle Time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internal clock/16	1.3		μs
			Internal clock/64	5.3		μs
Serial Clock Low-Level Range	t_{WSKL}	Input	External clock	420		ns
		Output	Internal clock/16	556		ns
			Internal clock/64	2.5		μs
Serial Clock High-Level Range	t_{WSKH}	Input	External clock	420		ns
		Output	Internal clock/16	556		ns
			Internal clock/64	2.5		μs
SI, SB0 Set-Up Time (Against $\overline{SCK}$ ↑)	t_{SSSK}			150		ns
SI, SB0 Hold Time (Against $\overline{SCK}$ ↑)	t_{HSSK}			400		ns
SO/SB0 Output Delay Time (Against $\overline{SCK}$ ↓)	t_{DSSSK1}	CMOS push-pull output (3-line serial I/O mode)		0	300	ns
	t_{DSSSK2}	Open-drain output (SBI mode), R_L = 1 KΩ		0	800	ns
SB0 High Hold Time (Against $\overline{SCK}$ ↑)	t_{HSSSK}	SBI mode		4		t_{CYX}
SB0 Low Set-Up Time (Against $\overline{SCK}$ ↓)	t_{SSSSK}			4		t_{CYX}
SB0 Low-Level Range	t_{WSSL}			4		t_{CYX}
SB0 High-Level Range	t_{WSSH}			4		t_{CYX}

Remarks : Values in the table are for f_{XX} = 12 MHz, C_L = 100 pF.

OTHER OPERATION

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI Low-Level Range	t_{WNIL}		10		μs
NMI High-Level Range	t_{WNIH}		10		μs
INTP0-INTP6 Low-Level Range	t_{WITL}		24		t_{CYX}
INTP0-INTP6 High-Level Range	t_{WITH}		24		t_{CYX}
$\overline{\text{RESET}}$ Low-Level Range	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ High-Level Range	t_{WRSH}		10		μs

EXTERNAL CLOCK TIMING

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
X1 Input Low-Level Range	t_{WXL}		30	130	ns
X1 Input High-Level Range	t_{WXH}		30	130	ns
X1 Input Rise Time	t_{XR}		0	30	ns
X1 Input Fall Time	t_{XF}		0	30	ns
X1 Input Clock Cycle Time	t_{CYX}		82	250	ns

COMPARATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = +5 V ±5 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Comparison Accuracy	V_{ACOMP}				100	mV
Comparison Time	t_{COMP}		128		256	t_{CYX}
Sampling Time	t_{SAMP}		62			t_{CYX}
PT Input Voltage	V_{IPT}		0		V_{DD}	V

DEFINITION OF BUS TIMING DEPENDING ON t_{CYX}

Parameter	Symbol	Calculation Formula	MIN./MAX.	12 MHz	Unit	
X1 Input Clock Cycle Time	t_{CYX}		MIN.	82	ns	
Address Set-Up Time (Against ASTB ↓)	t_{AAST}	$t_{CYX} - 30$	MIN.	52	ns	
Address → $\overline{RD}$ ↓ Delay Time	t_{DAR}	$2t_{CYX} - 35$	MIN.	129	ns	
Address Float Time (Against $\overline{RD}$ ↓)	t_{FAR}	$t_{CYX}/2 - 30$	MIN.	11	ns	
Address → Data Input Time	t_{DAID}	$(4 + 2n)\ t_{CYX} - 100$	MAX.	228•	ns	
ASTB ↓ → Data Input Time	t_{DSTID}	$(3 + 2n)\ t_{CYX} - 65$	MAX.	181•	ns	
$\overline{RD}$ ↓ → Data Input Time	t_{DRID}	$(2 + 2n)\ t_{CYX} - 64$	MAX.	100•	ns	
ASTB ↓ → $\overline{RD}$ ↓ Delay Time	t_{DSTR}	$t_{CYX} - 30$	MIN.	52	ns	
$\overline{RD}$ ↑ → Address Active Time	t_{DRA}	$2t_{CYX} - 40$	MIN.	124	ns	
$\overline{RD}$ ↑ → ASTB ↑ Delay Time	t_{DRST}	$2t_{CYX} - 40$	MIN.	124	ns	
$\overline{RD}$ Low-Level Range	t_{WRL}	$(2 + 2n)\ t_{CYX} - 40$	MIN.	124•	ns	
ASTB High-Level Range	t_{WSTH}	$t_{CYX} - 30$	MIN.	52	ns	
Address → $\overline{WR}$ ↓ Delay Time	t_{DAW}	$2t_{CYX} - 35$	MIN.	129	ns	
ASTB ↓ → Data Output Time	t_{DSTOD}	$t_{CYX} + 60$	MAX.	142	ns	
ASTB ↓ → $\overline{WR}$ ↓ Delay Time	t_{DSTW1}	$t_{CYX} - 30$ (Refresh disabled)	MIN.	52	ns	★
	t_{DSTW2}	$2t_{CYX} - 35$ (Refresh enabld)	MIN.	129	ns	
Data Set-Up Time (Against $\overline{WR}$ ↑)	t_{SODWR}	$(3 + 2n)\ t_{CYX} - 100$	MIN.	146•	ns	
Data Set-Up Time (Against $\overline{WR}$ ↓)	t_{SODWF}	$t_{CYX} - 60$ (Refresh enabled)	MIN.	22	ns	
$\overline{WR}$ ↑ → ASTB ↑ Delay Time	t_{DWST}	$t_{CYX} - 40$	MIN.	42	ns	
$\overline{WR}$ Low-Level Range	t_{WWL1}	$(3 + 2n)\ t_{CYX} - 50$ (Refresh disabled)	MIN.	196•	ns	★
	t_{WWL2}	$(2 + 2n)\ t_{CYX} - 50$ (Refresh enabled)	MIN.	114•	ns	
Address → $\overline{WAIT}$ ↓ Input Time	t_{DAWT}	$3t_{CYX} - 100$	MAX.	146	ns	
ASTB ↓ → $\overline{WAIT}$ ↓ Input Time	t_{DSTWT}	$2t_{CYX} - 80$	MAX.	84	ns	

• : When n = 0

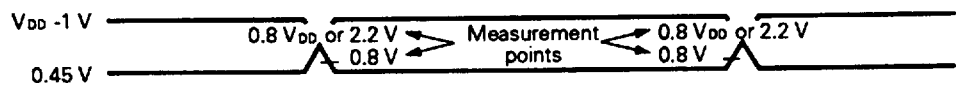
Remarks : n indicates the number of WAIT states.

DATA RETENTION CHARACTERISTICS (T_a = –40 to +85 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data Retention Current	I_{DDDR}	V_{DDDR} = 2.5 V		2	20	μA
		V_{DDDR} = 5 V ± 10 %		5	50	μA
V_{DD} Rise Time	t_{RVD}		200			μs
V_{DD} Fall Time	t_{FVD}		200			μs
V_{DD} Retention Time (for STOP Mode Setting)	t_{HVD}		0			ms
STOP Release Signal Input Time	t_{DREL}		0			ms
Oscillation Stabilization Wait Time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-Level Input Voltage	V_{IL}	Specified pins*	0		0.1 V_{DDDR}	V
High-Level Input Voltage	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

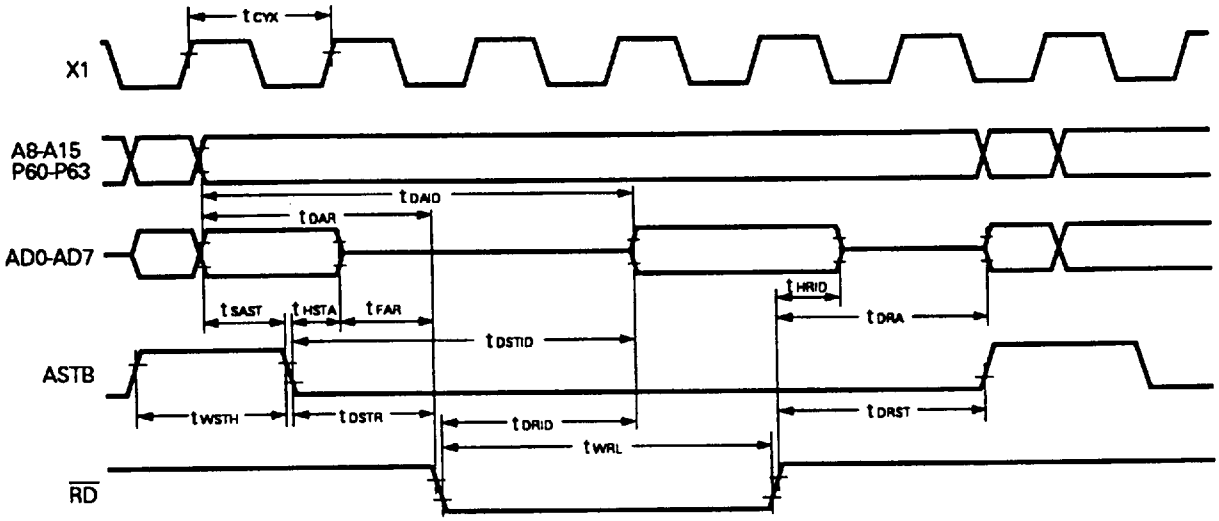
* : $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, and $\overline{\text{EA}}$ pins.

AC TIMING MEASUREMENT POINTS

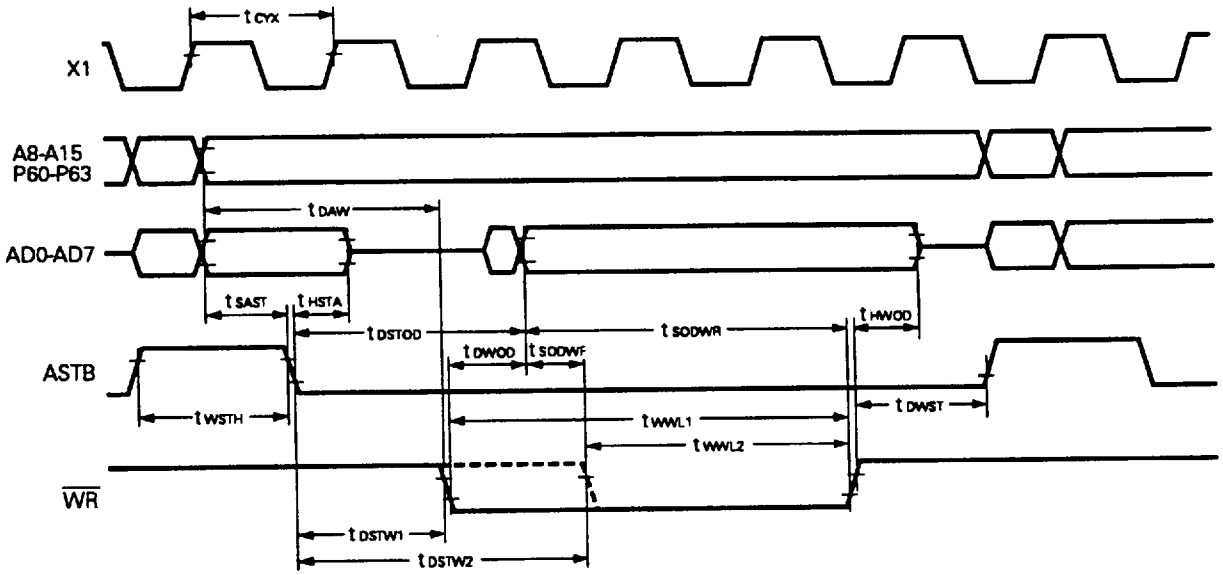


TIMING WAVE-FORMS

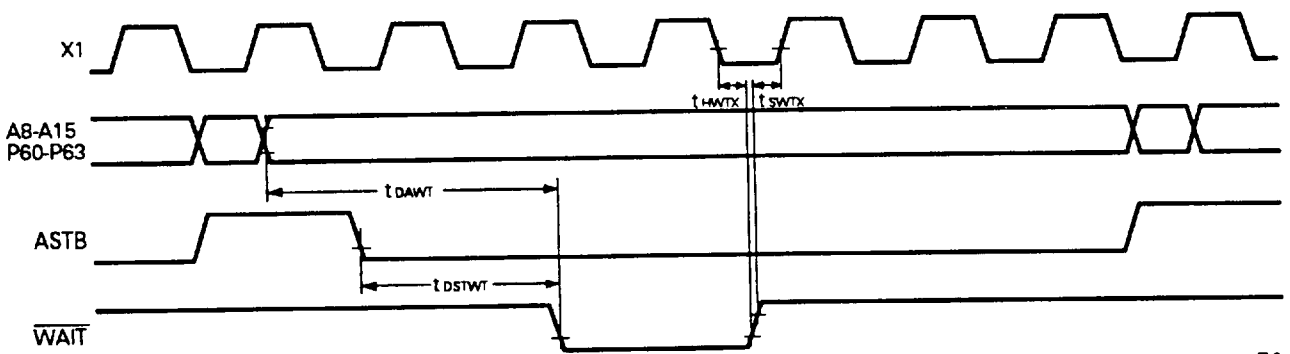
READ OPERATION



WRITE OPERATION

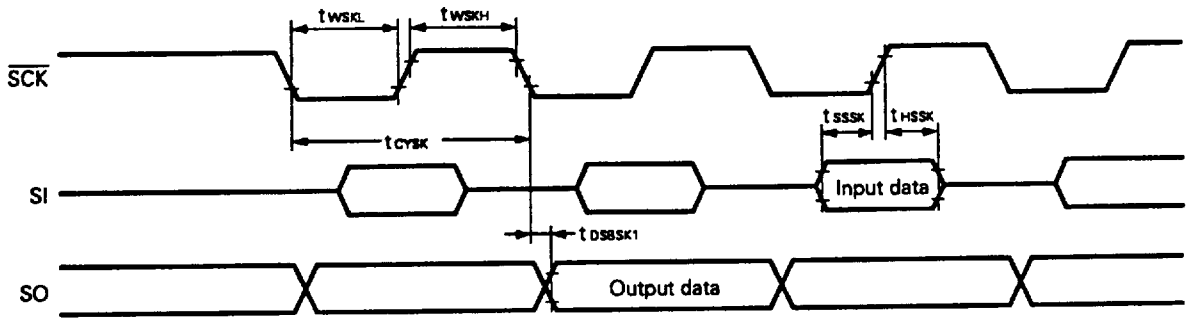


EXTERNAL WAIT INPUT TIMING



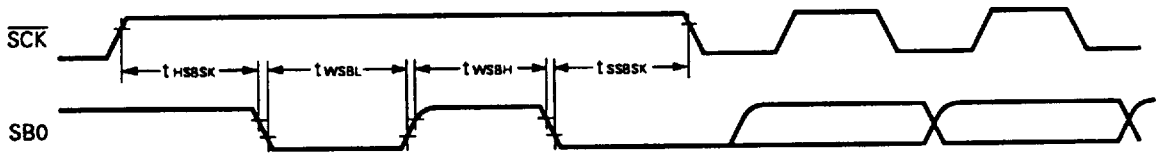
SERIAL OPERATION

3-LINE SERIAL I/O MODE

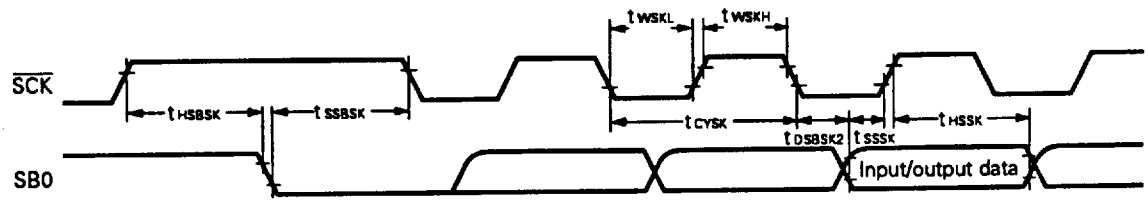


SBI MODE

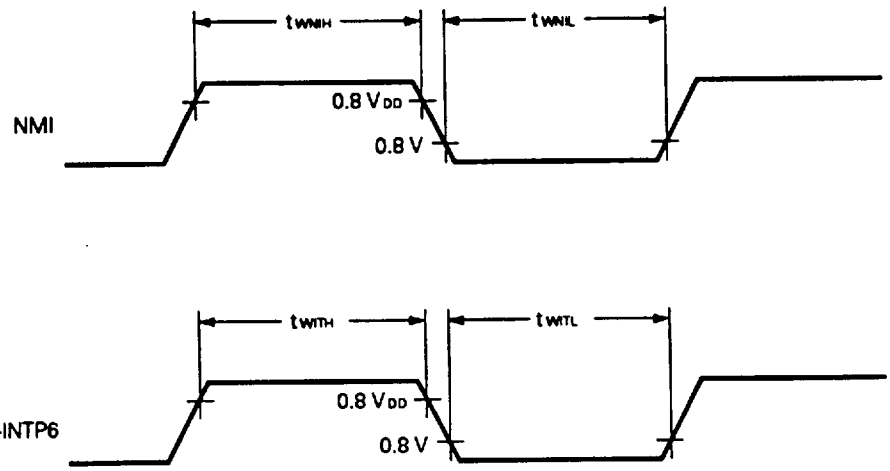
BUS RELEASE SIGNAL TRANSFER



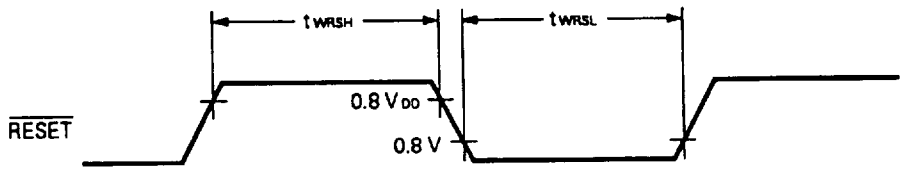
COMMAND SIGNAL TRANSFER



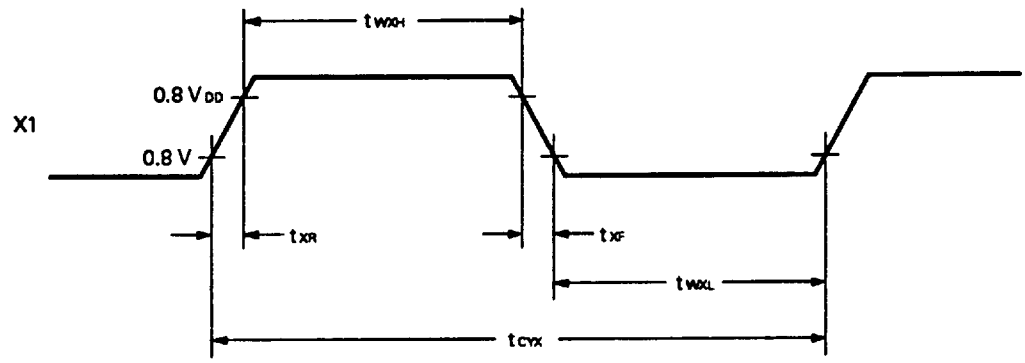
INTERRUPT INPUT TIMING



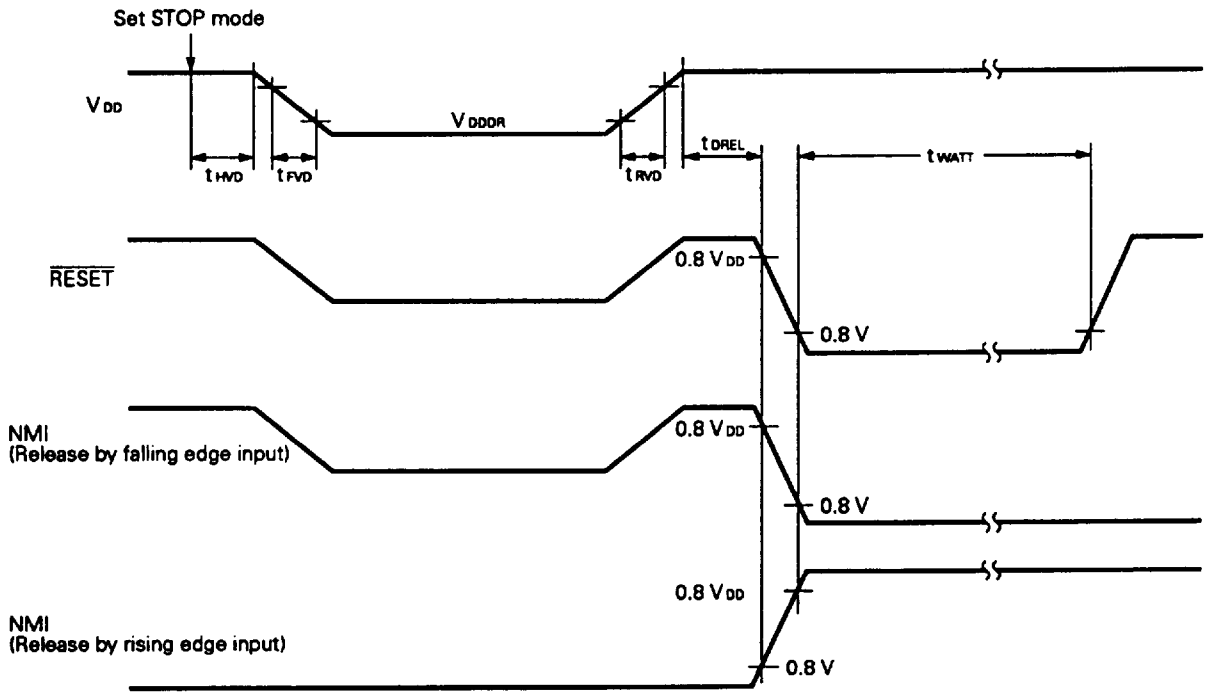
RESET INPUT TIMING



EXTERNAL CLOCK TIMING

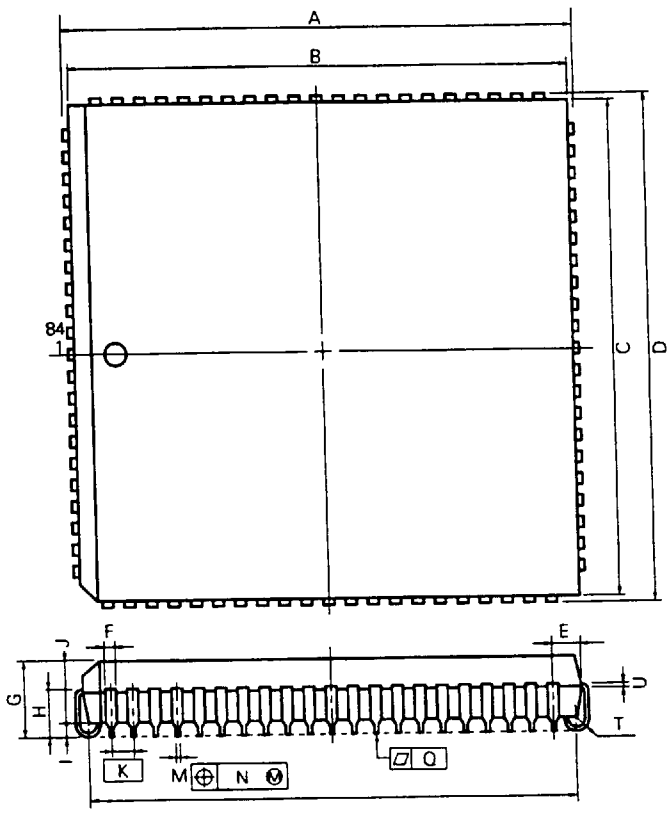


DATA RETENTION CHARACTERISTICS



9. PACKAGE DRAWINGS

84 PIN PLASTIC QFJ (□1150 mil)

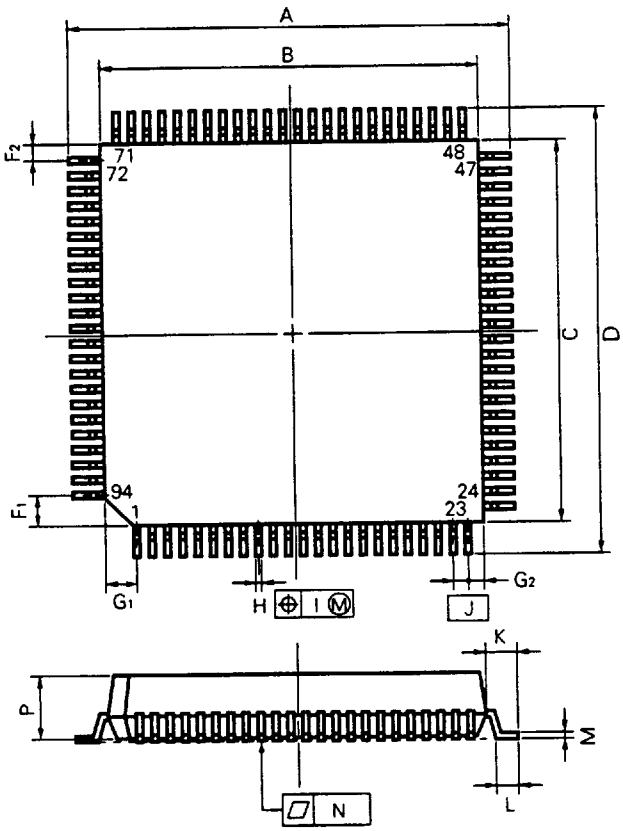


P84L-50A3-2

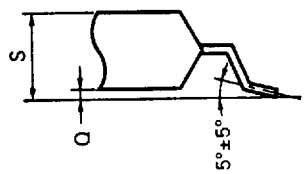
NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	30.2±0.2	1.189±0.008
B	29.28	1.153
C	29.28	1.153
D	30.2±0.2	1.189±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	28.20±0.20	$1.110^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

94 PIN PLASTIC QFP (□20)



detail of lead end



S94GJ-80-5BG-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.4	$0.913^{+0.017}_{-0.016}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	23.2±0.4	$0.913^{+0.017}_{-0.016}$
F_1	1.6	0.063
F_2	0.8	0.031
G_1	1.6	0.063
G_2	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
S	4.0 MAX.	0.158 MAX.

10. RECOMMENDED SOLDERING CONDITIONS

For the μPD78220/μPD78224, soldering must be performed under the following conditions.

For details of recommended condtions for surface mounting, refer to information document "Surface mount device mounting manual" (IEI-616).

For other soldering methods, please consult with NEC sales personnel.

Table 10-1 Surface Mounting Type Soldering Conditions

(1) μPD78220GJ-5BG, 78224GJ-XXX-5BG: 94-pin plastic QFP (□ 20 mm)

Soldering Method	Solering Conditions	Recommended Condition Reference Code
Infrared Reflow	Package peak temperature: 230 °C, Time: 30 seconds max. (more than 210 °C), Number of soldering operations: 1, Maximum number of days: 7 days*1 (Afterwards, 10 hours prebaking at 125 °C is required)	IR30-107-1*2
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (more than 200 °C), Number of soldering operations: 1, Maximum number of days: 7 days*1 (Afterwards, 10 hours prebaking at 125 °C is required)	VP15-107-1*2
Wave Soldering	Solder bath temperature: 260 °C, Time: 10 seconds max., Number of soldering operations: 1, Pre-heating temperature: 120 °C max. (Package surface temperature), Maximum number of days: 7 days*1 (Afterwards, 10 hours prebaking at 125 °C is required)	WS60-107-1*2
Pin Partial Heating	Pin temperature: 300 °C max., Time: 3 seconds max. (Per side)	—

(2) μPD78220L, 78224L-XXX: 84-pin plastic QFJ (□ 1150 mil)

Soldering Method	Solering Conditions	Recommended Condition Reference Code
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (more than 200 °C), Number of soldering operations: 1, Maximum number of days: 2 days*1 (Afterwards, 16 hours prebaking at 125 °C is required)	VP15-162-1
Pin Partial Heating	Pin temperature: 300 °C max., Time: 3 seconds max. (Per side)	—

*1 : This means the number of days after unpacking the dry pack. Storage conditions are 25 °C and 65 % RH max.

*2 : These conditions are not applicable to the "P" standard and "X" standard products.

Caution : Do not use one soldering method in combination with another. (however, pin partial heating can be performed with other soldering methods).

Notice

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, numbr of times: 2, and an extended number of days) is also available.
For details, consult NEC.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for development of systems using the μPD78220 and 78224:

Language Processor

RA78K/II	*1, 2	Assembler package common to 78K/II series
CC78K/II	*1, 2	C compiler package common to 78K/II series
CC78K/II-L	*1, 2	C compiler library source file common to 78K/II series

PROM Writing Tools

PG-1500		PROM programmer
PA-78P224GJ PA-78P224L		Programmer adapter connected to PG-1500
PG-1500 Controller	*1	Control program for PG-1500

Debugging Tools

IE-78230-R-A IE-78230-R IE-78220-R	 *3 *3	In-circuit emulator common to μPD78224 series
IE-78200-R-BK		Break board common to 78K/II series
IE-78220-R-EM IE-78230-R-EM IE-78200-R-EM	*3 *3	Emulation board for μPD78224 series
EP-78220GJ EP-78230GJ-R EP-78220L EP-78230LQ-R	*3 *3 	Emulation probe common to μPD78224 series
EV-9200G-94		Socket mounted to user system created for 94-pin plastic QFP
SD78K/II	*1	Screen debugger for IE-78230-R-A
DF78220	*1	Device file for μPD78224 series

Real-Time OS

RX78K/II	*1, 2	Real-time OS common to 78K/II series

Fuzzy Inference Development Support Systems

FE9000	*1	Fuzzy knowledge data creation tool
FT9080	*1	Translator
FI78K/II	*1	Fuzzy inference module
FD78K/II	*1, 4	Fuzzy inference debugger

*1: PC-9800 series (MS-DOS™) base, IBM PC/AT™ (PC DOS™) base
2: HP9000 series 300™ (HP-UX™) base, SPARCstation™ (Sun OS™) base, EWS-4800 series™ (EWS-UX/V™) base
3: This model is not produced any more.
4: Under development

Remarks: For development tools from other companies, refer to 78K/II Series Development Tool Selection Guide (EF-231).

★ APPENDIX B. RELATED DOCUMENTS

[MEMO]

GENERAL NOTES ON CMOS DEVICES

① STATIC ELECTRICITY (ALL MOS DEVICES)

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to "Processing of Unused Pins" in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

[MEMO]

NEC
NEC Electronics Inc.
CORPORATE HEADQUARTERS*
2880 Scott Boulevard
P.O. Box 58062
Santa Clara, CA 95052-8062
TEL 408-588-6000
* As of September 3, 1996

For literature, call toll-free 7 a.m. to 6 p.m. Pacific time: **1-800-366-9782**
or FAX your request to: **1-800-729-9288**

IC-2374D