

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC4020AP, TC74HC4020AF, TC74HC4020AFN
TC74HC4040AP, TC74HC4040AF, TC74HC4040AFN
TC74HC4020AP/AF/AFN 14 - STAGE BINARY COUNTER
TC74HC4040AP/AF/AFN 12 - STAGE BINARY COUNTER

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74HC4020A / TC74HC4040A are high speed CMOS BINARY COUNTER / DIVIDERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS dissipation.

The TC74HC4020A is a 14 - STAGE BINARY COUNTER, and the TC74HC4040A is a 12 - STAGE BINARY COUNTER. Setting CLR to high resets the counter to low.

A negative transition on the CK input brings one increment into the counter.

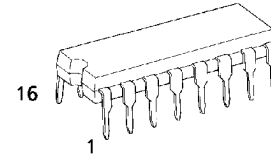
The TC74HC4020A provides 12 divided outputs : 1'st stage and atage 4 thru stage 14. At Q14, a 1 / 16384 divided frequency will be output.

The TC74HC4040A provides all divided output stages, and at Q12, a 1 / 4096 divided frequency will be output.

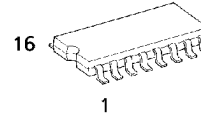
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

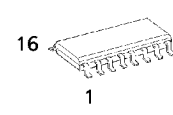
- High Speed..... $f_{MAX} = 73\text{MHz}$ (typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..... $|I_{OH}| = |I_{OL}| = 4\text{mA}$ (Min.)
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range..... V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 4020B / 4040B



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

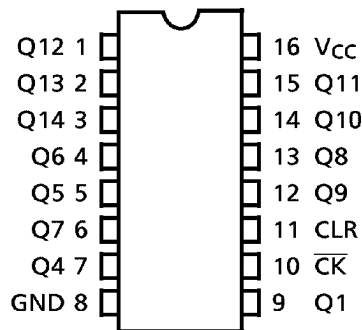
TRUTH TABLE

$\overline{\text{CK}}$	CLR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
	L	NO CHANGE
	L	ADOVANCE TO NEXT STATE

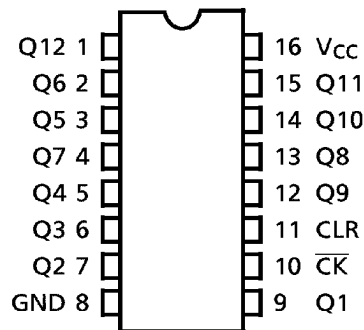
X : Don't Care

PIN ASSIGNMENT

TC74HC4020A



TC74HC4040A



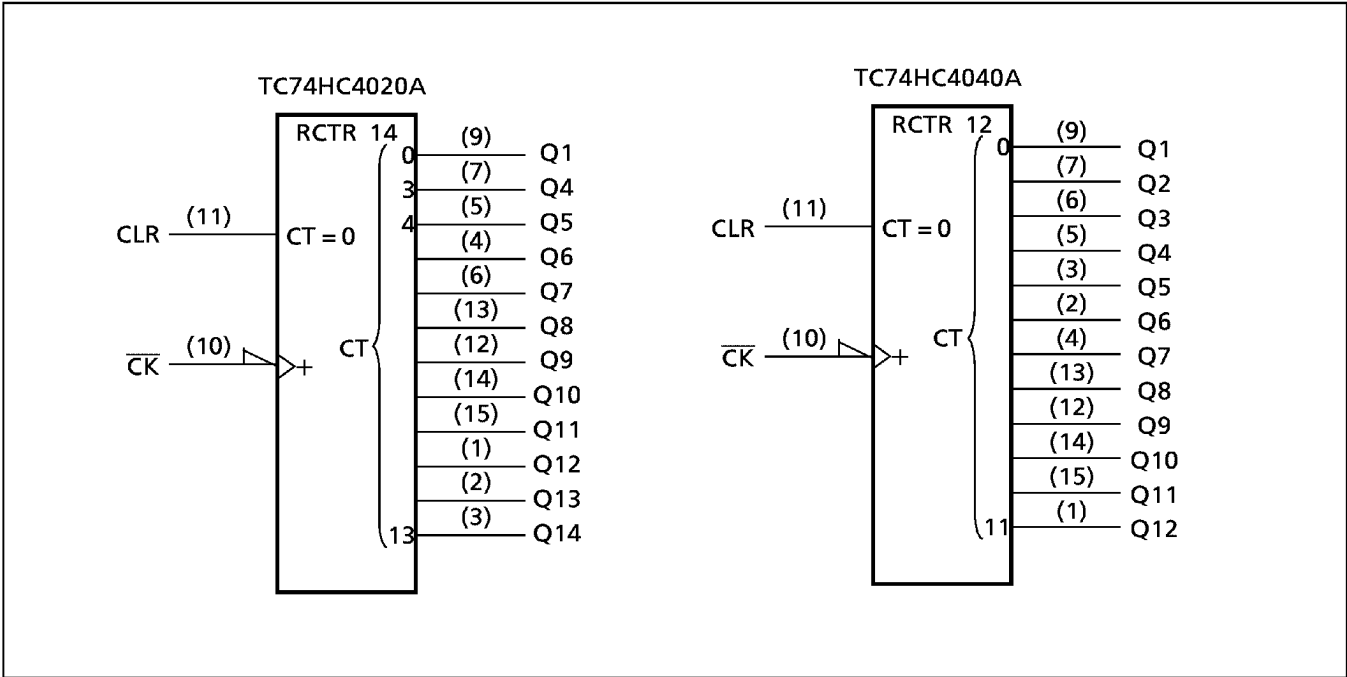
(TOP VIEW)

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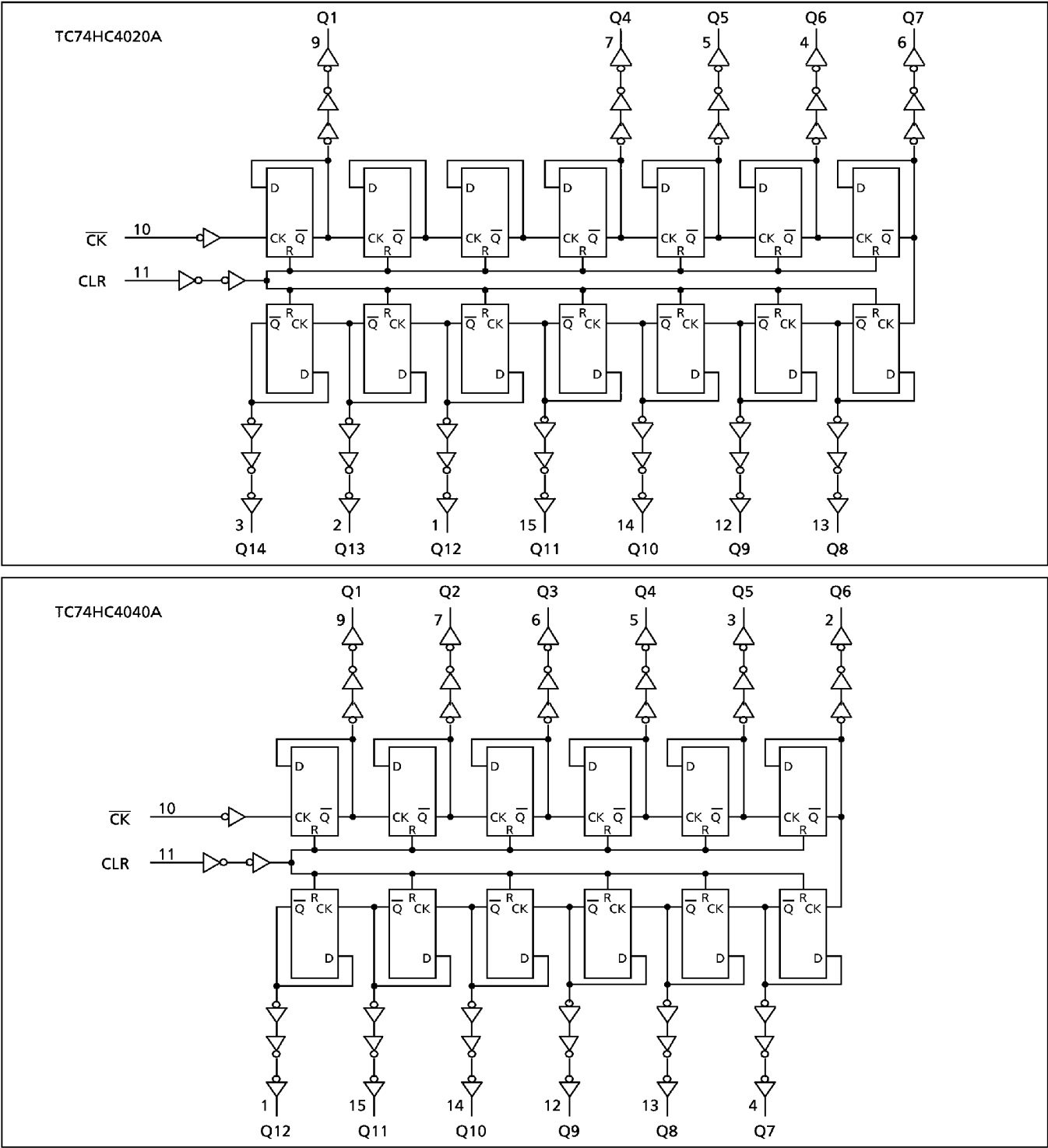
IEC LOGIC SYMBOL



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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	V
			$I_{OH} = -4 \text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80	—	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			$I_{OL} = 4 \text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	
			$I_{OL} = 5.2 \text{ mA}$	6.0	—	0.18	0.26	—	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{CK}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CLR)	$t_{W(H)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Removal Time	t_{rem}		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	30	24	
			6.0	—	35	28	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CK—Q1)	t_{pLH} t_{pHL}		—	16	24	
Propagation Delay Time (Qn—Qn+1)	Δt_{pd}		—	5	14	
Propagation Delay Time (CLR)	t_{pHL}		—	14	24	
Maximum Clock Frequency	f_{MAX}		33	73	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation Delay Time (CK—Q1)	t_{pLH} t_{pHL}		2.0	—	70	145	—	180
			4.5	—	20	29	—	36
			6.0	—	17	25	—	31
Propagation Delay Time (Qn—Q+1)	Δt_{pd}		2.0	—	20	75	—	95
			4.5	—	6	15	—	19
			6.0	—	4	13	—	16
Propagation Delay Time (CLR)	t_{pHL}		2.0	—	55	140	—	175
			4.5	—	17	28	—	35
			6.0	—	14	24	—	30
Maximum Clock Frequency	f_{MAX}		2.0	6	17	—	5	—
			4.5	30	66	—	24	—
			6.0	35	78	—	28	—
Input Capacitance	C_{IN}			—	5	10	—	10
Power Dissipation Capacitance	C_{PD} (1)	TC74HC4020A		—	27	—	—	—
		TC74HC4040A		—	37	—	—	—

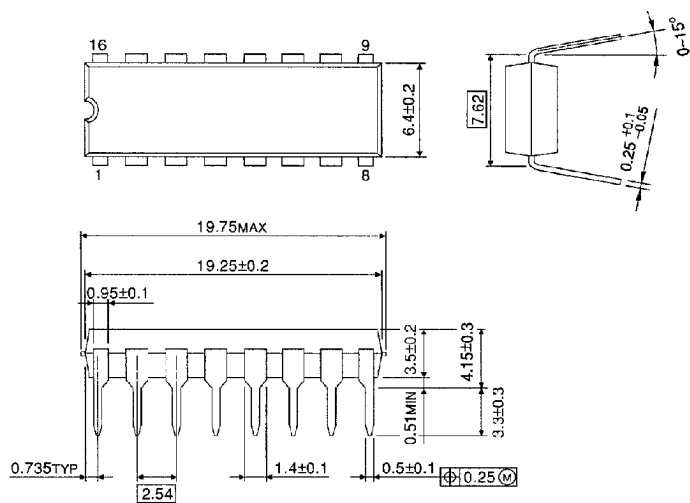
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

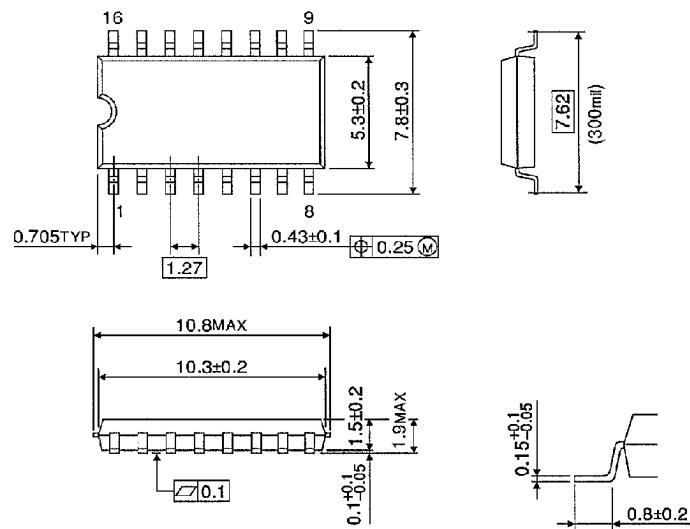
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

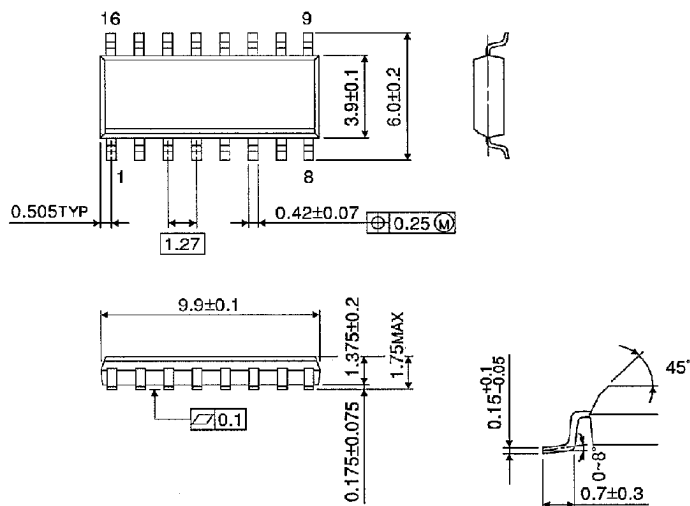


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)