

TrenchMOS™ transistor

Standard level FET

PHB37N06T

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in DC-DC converters and general purpose switching applications.

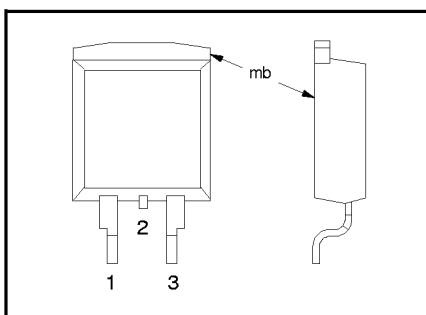
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	37	A
P_{tot}	Total power dissipation	100	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10\text{ V}$	35	mΩ

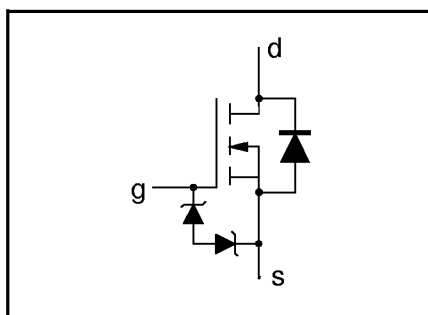
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	$T_{mb} = 25\text{ °C}$	-	37	A
I_D	Drain current (DC)	$T_{mb} = 100\text{ °C}$	-	26	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\text{ °C}$	-	148	A
P_{tot}	Total power dissipation	$T_{mb} = 25\text{ °C}$	-	100	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	1.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

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STATIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}; T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}; T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	2.0 1.0	3.0 -	4.0 -	V V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V}; T_j = 175^\circ\text{C}$	-	0.05	10	μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}; T_j = 175^\circ\text{C}$	-	0.04	500	μA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	$I_G = \pm 1\text{ mA}; T_j = 175^\circ\text{C}$	-	-	20	μA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 17\text{ A}; T_j = 175^\circ\text{C}$	16	28	35	m Ω
			-	-	74	m Ω

DYNAMIC CHARACTERISTICS

 $T_{mb} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 15\text{ A}$	4	-	-	S
$Q_{g(tot)}$	Total gate charge	$I_D = 30\text{ A}; V_{DD} = 44\text{ V}; V_{GS} = 10\text{ V}$	-	26	-	nC
Q_{gs}	Gate-source charge		-	7.5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	11	-	nC
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	700	880	pF
C_{oss}	Output capacitance		-	200	40	pF
C_{rss}	Feedback capacitance		-	100	140	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 15\text{ A}; V_{GS} = 10\text{ V}; R_G = 10\ \Omega$	-	11	16	ns
t_r	Turn-on rise time		-	35	50	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	25	35	ns
t_f	Turn-off fall time		-	22	29	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	37	A
I_{DRM}	Pulsed reverse drain current		-	-	148	A
V_{SD}	Diode forward voltage	$I_F = 25\text{ A}; V_{GS} = 0\text{ V}$ $I_F = 34\text{ A}; V_{GS} = 0\text{ V}$	-	0.95 1.0	1.2 -	V
t_{rr}	Reverse recovery time	$I_F = 34\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s}; V_{GS} = -10\text{ V}; V_R = 30\text{ V}$	-	40	-	ns
Q_{rr}	Reverse recovery charge		-	0.16	-	μC

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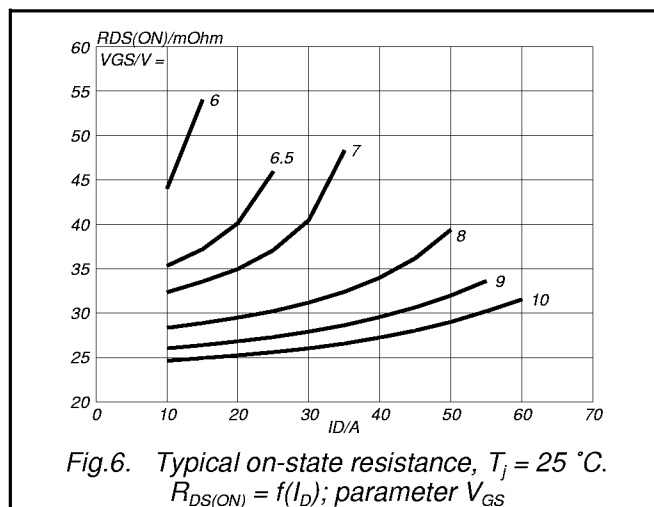
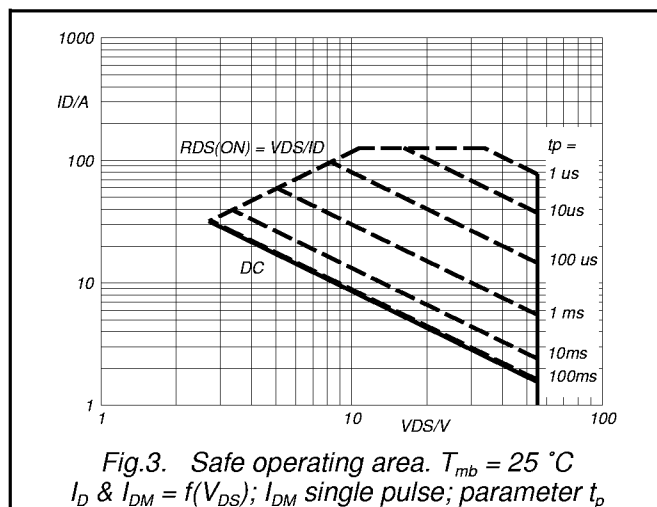
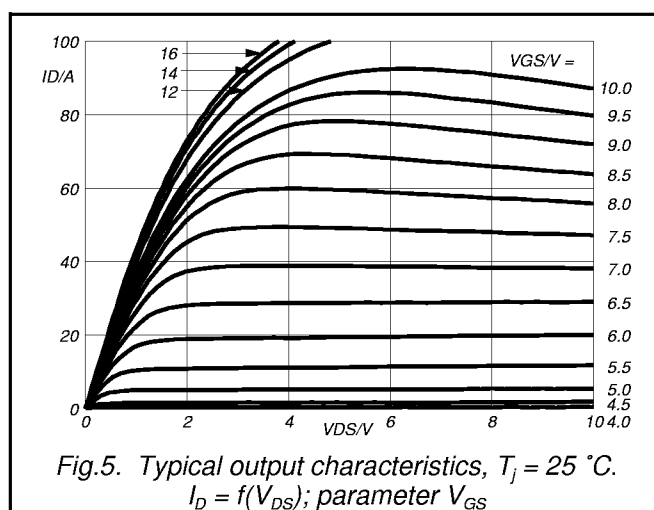
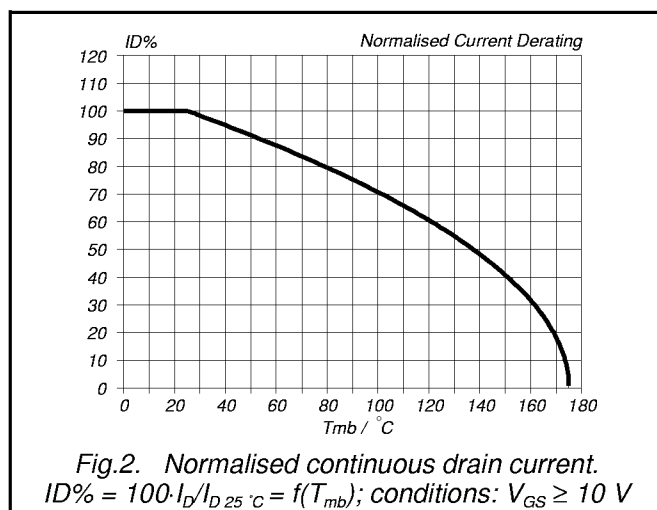
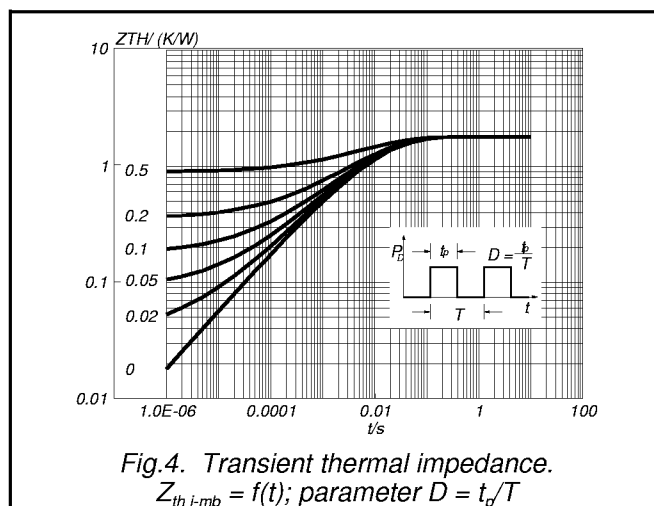
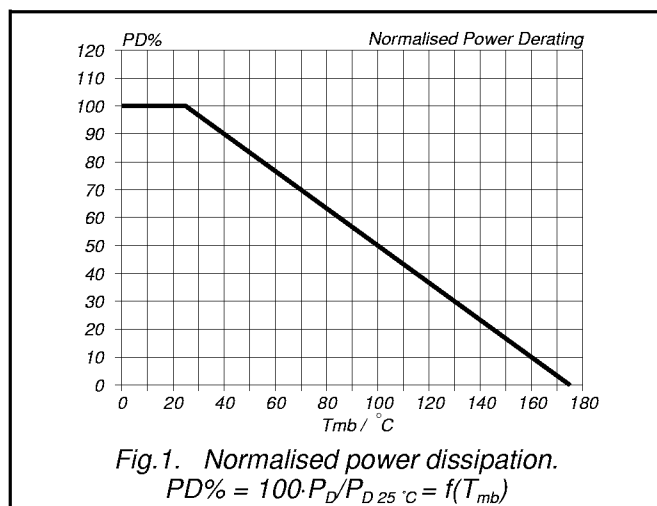
AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 20\text{ A}$; $V_{DD} \leq 25\text{ V}$; $V_{GS} = 10\text{ V}$; $R_{GS} = 50\ \Omega$; $T_{mb} = 25\text{ °C}$	-	-	45	mJ

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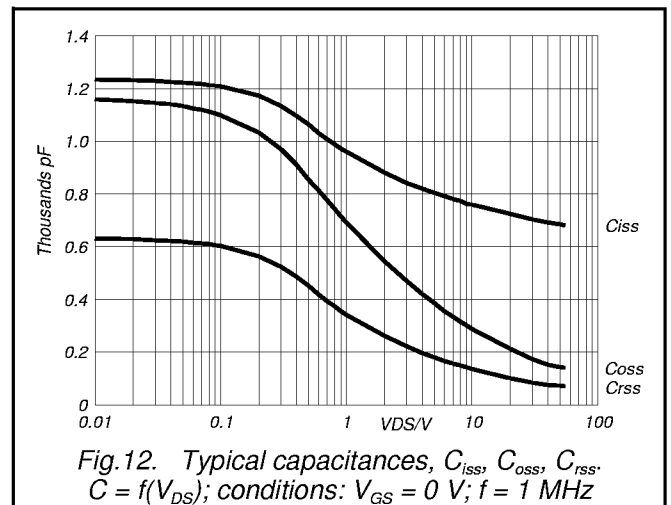
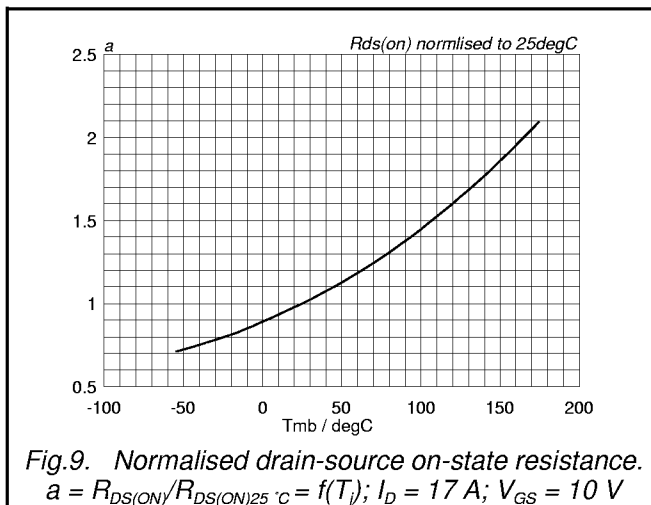
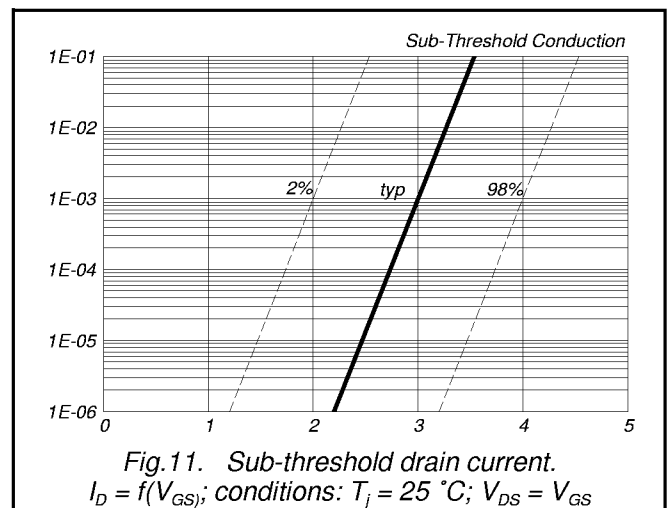
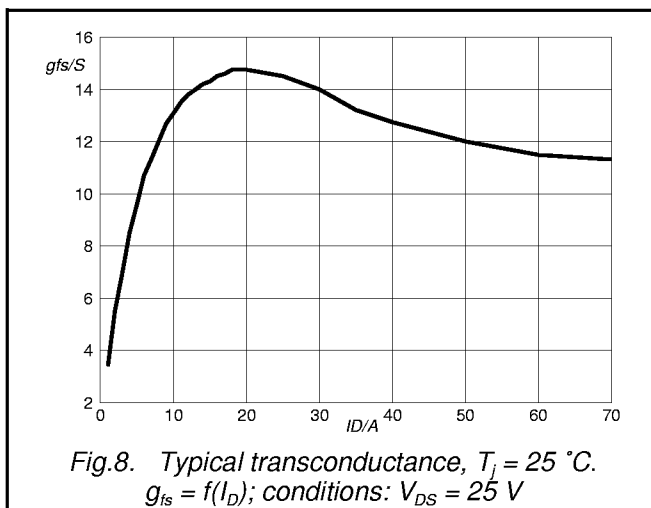
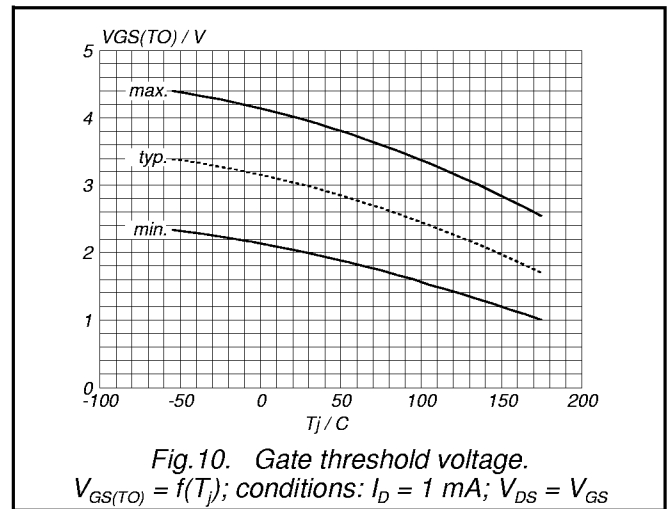
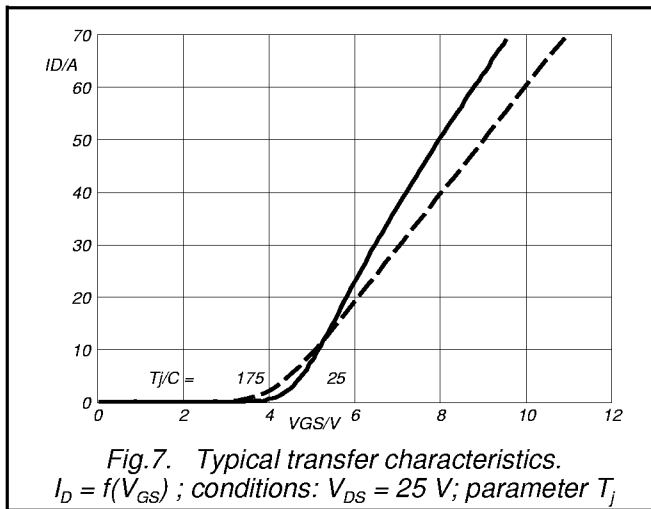
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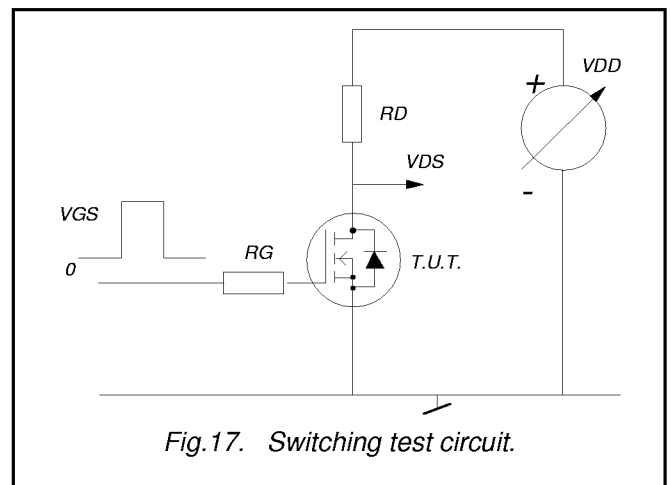
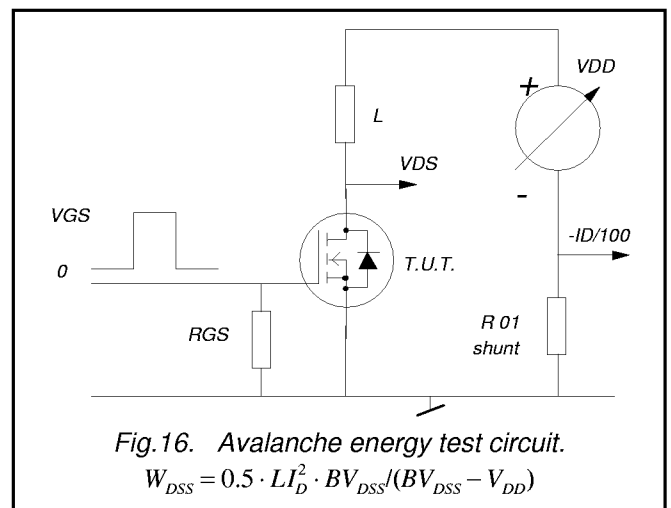
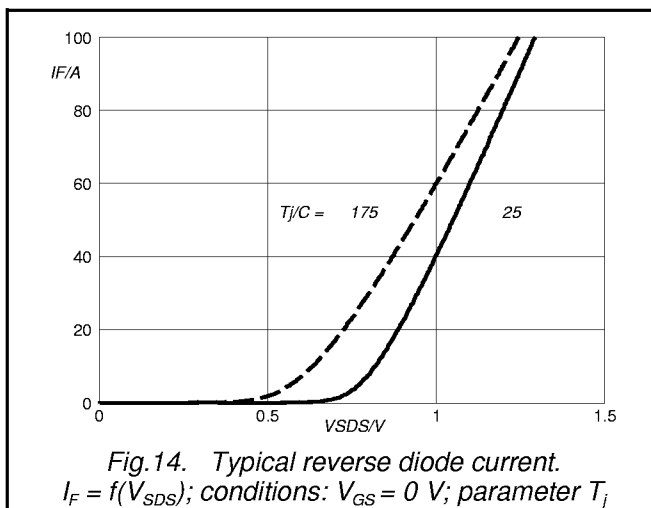
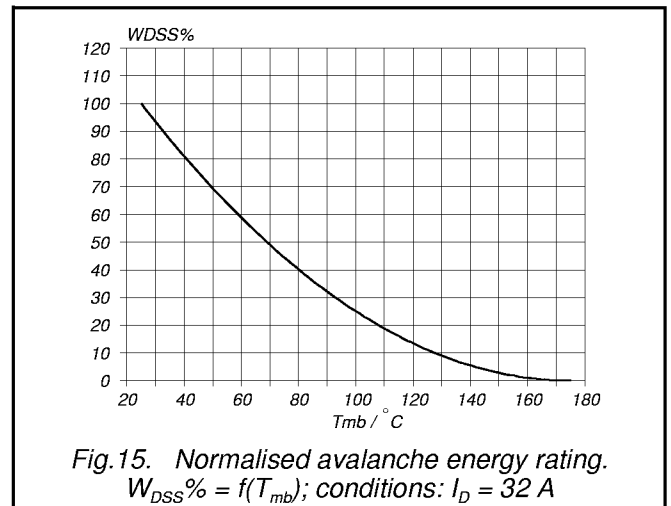
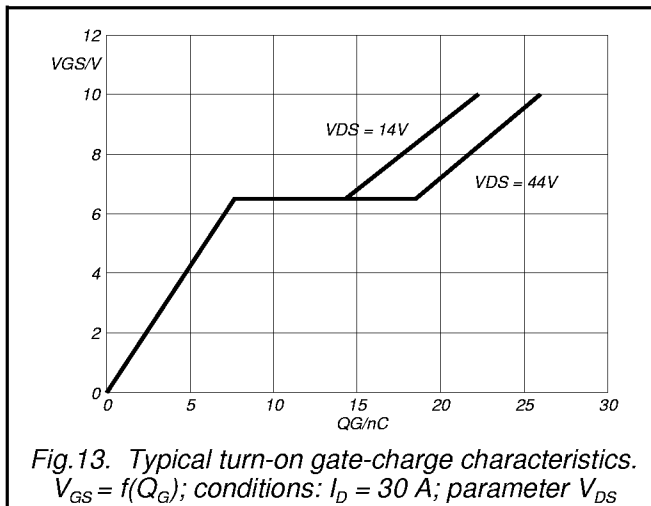
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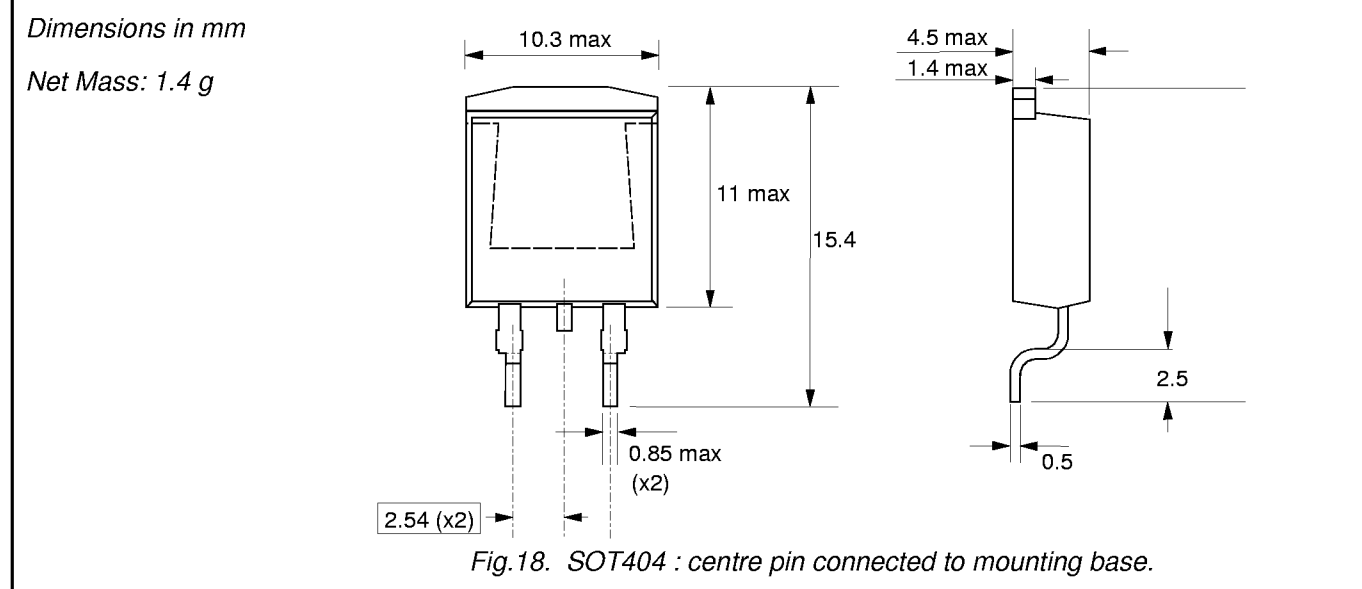


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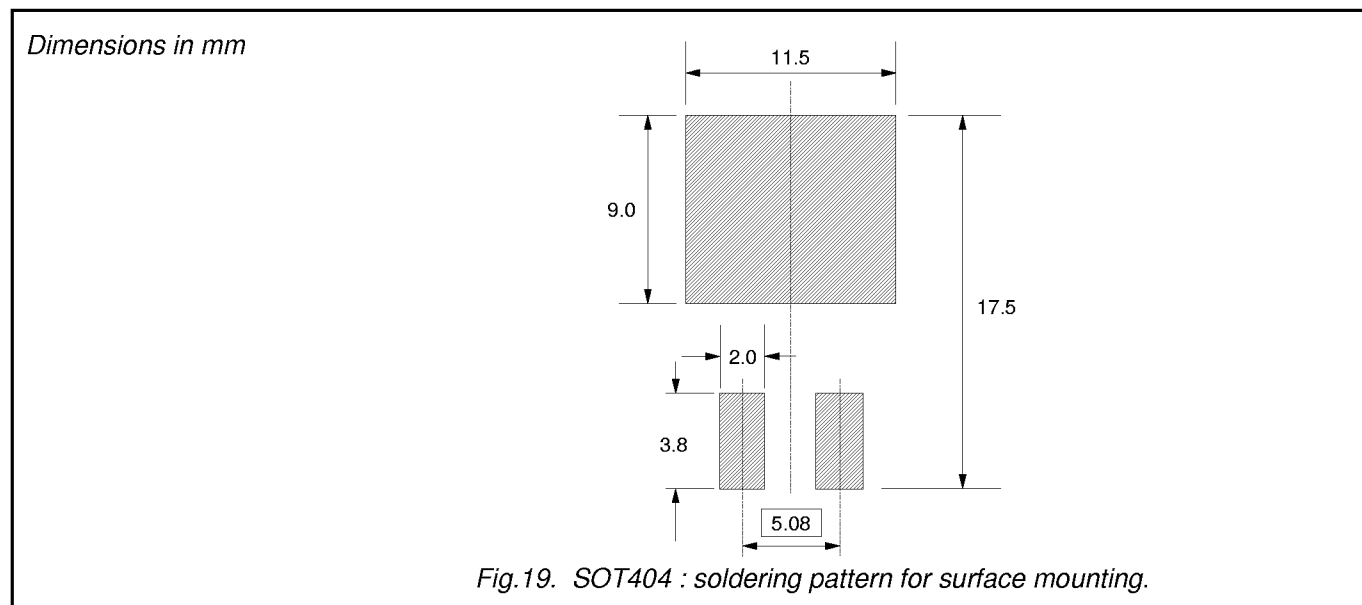
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MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".