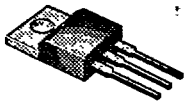
Siliconix incorporated

IRF720/721/722/723

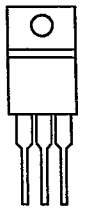
N-Channel Enhancement Mode Transistors

T-39-11

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

1 2 3

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
IRF720	400	1.8	3.0
IRF721	350	1.8	3.0
IRF722	400	2.5	2.5
IRF723	350	2.5	2.5

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	IRF 720	IRF 721	IRF 722	IRF 723	UNITS
Gate-Source Voltage		V_{GS}	±20	±20	±20	±20	V
Continuous Drain Current	T_C = 25°C	I_D	3.0	3.0	2.5	2.5	A
	T_C = 100°C		2.0	2.0	1.5	1.5	
Pulsed Drain Current[1]		I_{DM}	12	12	10	10	
Avalanche Current (See Figure 9)		I_{AR}	3.0	3.0	3.0	3.0	
Repetitive Avalanche Energy[2]	L = 1.0 mH	E_{AR}	4.5	4.5	4.5	4.5	mJ
Power Dissipation	T_C = 25°C	P_D	40	40	40	40	W
	T_C = 100°C		16	16	16	16	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300				

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		3.12	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

IRF720/721/722/723

T-39-11

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER		SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	IRF720, 722 IRF721, 723	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		400 350		V
Gate Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage		I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
			V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	IRF720, 721 IRF722, 723	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		3.0 2.5		A
Drain-Source On-State Resistance[1]	IRF720, 721 IRF722, 723	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 1.5 A	1.5 1.8		1.8 2.5	Ω
	IRF720, 721 IRF722, 723		V_{GS} = 10 V, I_D = 1.5 A T_J = 125°C	3.0 3.5		3.5 4.9	
Forward Transconductance[1]		g_{fs}	V_{DS} = 15 V, I_D = 1.5 A	1.4	1.0		S
DYNAMIC							
Input Capacitance		C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	385		600	pF
Output Capacitance		C_{oss}		80		200	
Reverse Transfer Capacitance		C_{rss}		20		40	
Total Gate Charge[2]		Q_g	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4 A	17		18	nC
Gate-Source Charge[2]		Q_{gs}		3			
Gate-Drain Charge[2]		Q_{gd}		8			
Turn-On Delay Time[2]		$t_{d(on)}$	V_{DD} = 200 V, R_L = 130 Ω I_D ≃ 1.5 A, V_{GEN} = 10 V, R_G = 25 Ω	8		40	ns
Rise Time[2]		t_r		10		50	
Turn-Off Delay Time[2]		$t_{d(off)}$		42		100	
Fall Time[2]		t_f		20		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	IRF720, 721 IRF722, 723	I_S				3.0 2.5	A
Pulsed Current[3]	IRF720, 721 IRF722, 723	I_{SM}				12 10	
Forward Voltage[1]	IRF720, 721 IRF722, 723	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.6 1.5	V
Reverse Recovery Time		t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	250			ns
Reverse Recovery Charge		Q_{rr}		0.15			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

T-39-11

Figure 1. Output Characteristics

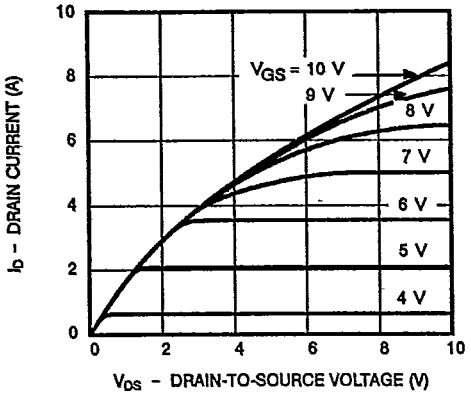


Figure 2. Transfer Characteristics

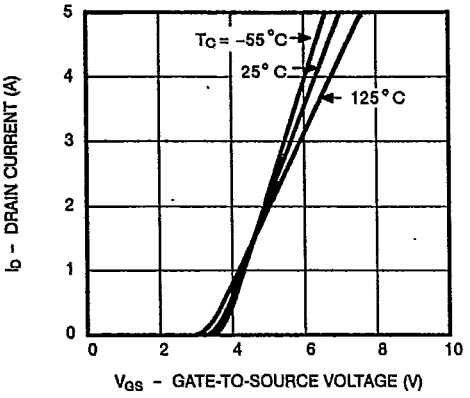


Figure 3. Transconductance

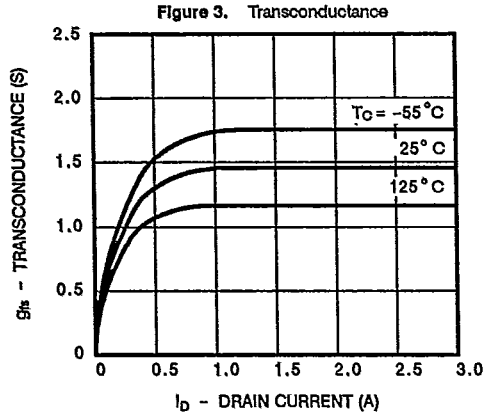


Figure 4. On-Resistance

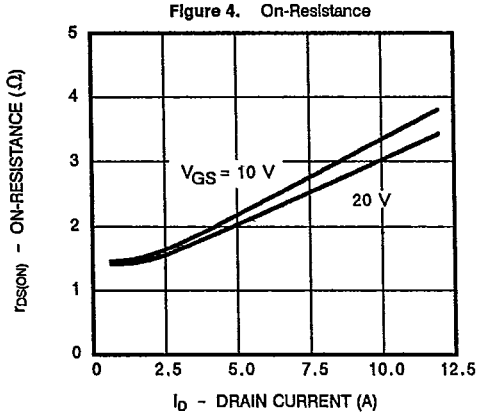


Figure 5. Capacitance

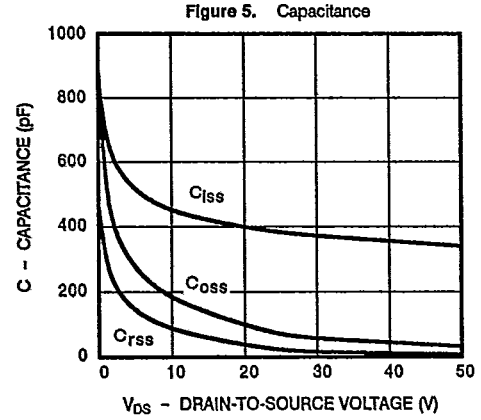
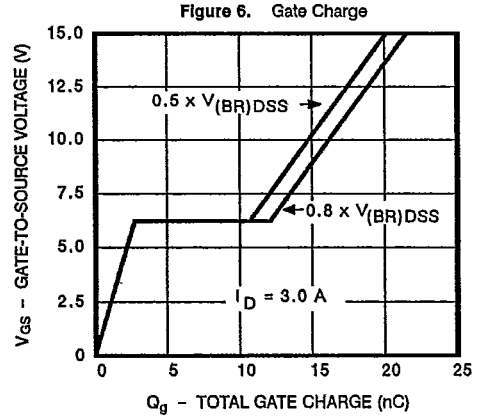


Figure 6. Gate Charge



IRF720/721/722/723

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TYPICAL CHARACTERISTICS (Cont'd)

T-39-11

Figure 7. On-Resistance vs. Junction Temperature

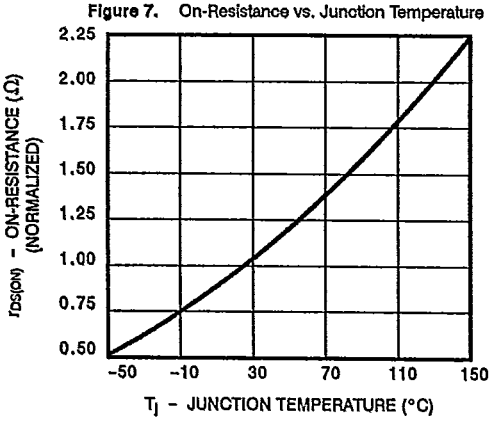
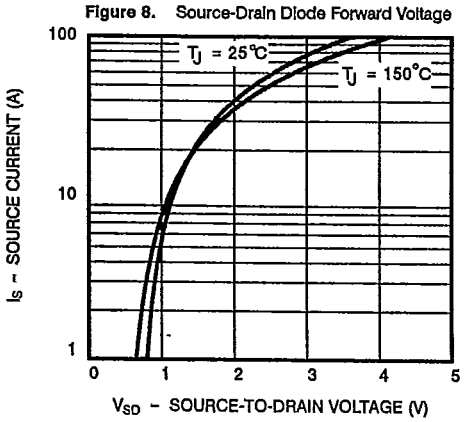


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

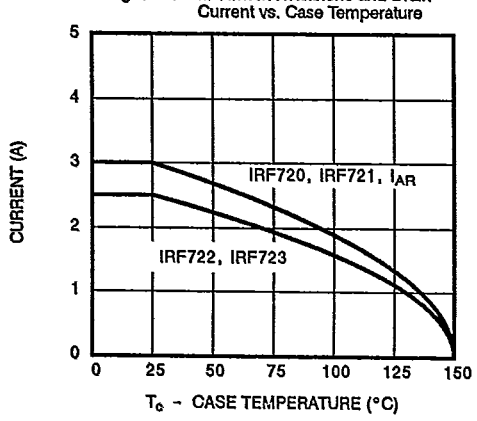
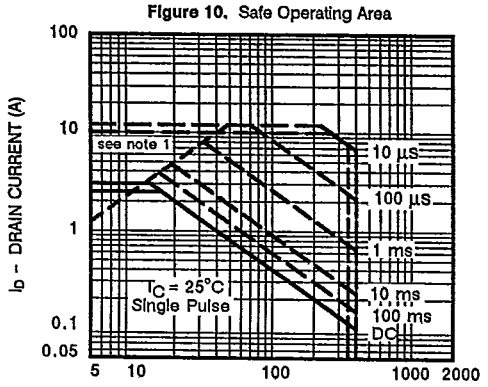


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case