

FDD6670A

N-Channel, Logic Level, PowerTrench® MOSFET

General Description

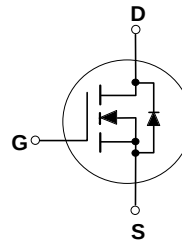
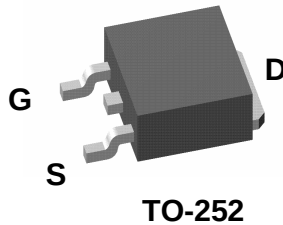
This N-Channel Logic level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- DC/DC converter
- Motor drives

Features

- 66 A, 30 V. $R_{DS(on)} = 0.008 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(on)} = 0.010 \Omega @ V_{GS} = 4.5 \text{ V}$.
- Low gate charge (35nC typical).
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(on)}$.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Maximum Drain Current -Continuous (Note 1) $T_A = 25^\circ\text{C}$ (Note 1a)	66	A
		15	
	Maximum Drain Current -Pulsed	100	
P_D	Maximum Power Dissipation $T_C = 25^\circ\text{C}$ (Note 1) $T_A = 25^\circ\text{C}$ (Note 1a)	70	W
		3.2	
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.3	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	1.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	$^\circ\text{C/W}$
	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD6670A	FDD6670A	13"	16mm	2500

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Drain-Source Avalanche ratings (Note 2)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 15\text{ V}$, $I_D = 66\text{ A}$			400	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				66	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		25		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}$, $V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	1.6	3	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		-4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$, $T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}$, $I_D = 13\text{ A}$		0.0065 0.0090 0.0085	0.008 0.013 0.010	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 5\text{ V}$	50			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 12\text{ A}$		55		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		3200		pF
C_{oss}	Output Capacitance			820		pF
C_{rss}	Reverse Transfer Capacitance			400		pF

Switching Characteristics (Note 2)

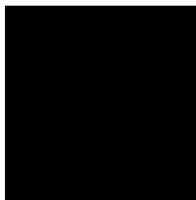
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		15	27	ns
t_r	Turn-On Rise Time			15	27	ns
$t_{d(off)}$	Turn-Off Delay Time			85	105	ns
t_f	Turn-Off Fall Time			42	68	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 5\text{ V}$		35	50	nC
Q_{gs}	Gate-Source Charge			9		nC
Q_{gd}	Gate-Drain Charge			16		nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current				2.3	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.3 A (Note 2)		0.72	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the drain tab. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



■ a) $R_{\theta JA} = 40^\circ\text{C/W}$ when mounted
 ■ on a 1 in^2 pad of 2oz copper.

■ b) $R_{\theta JA} = 96^\circ\text{C/W}$ when mounted
 ■ on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

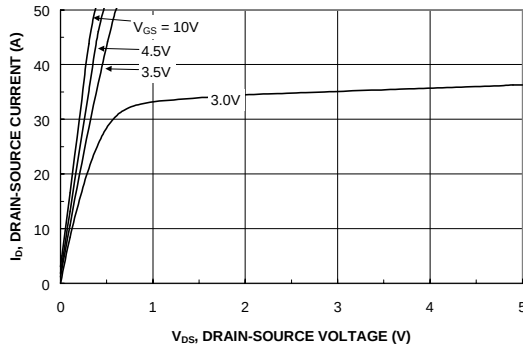


Figure 1. On-Region Characteristics.

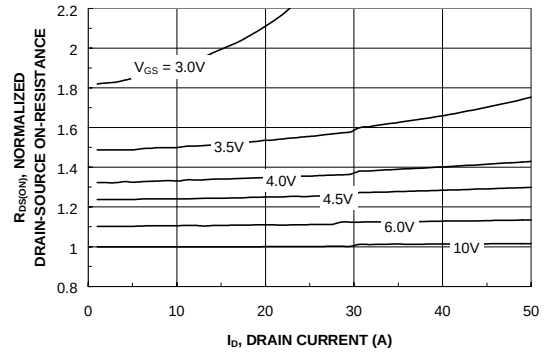


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

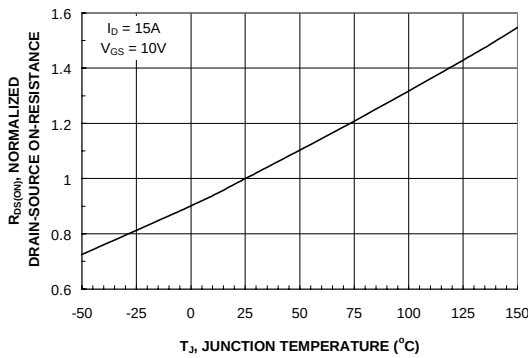


Figure 3. On-Resistance Variation with Temperature.

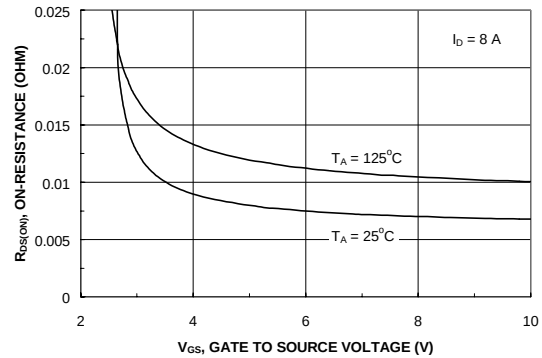


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

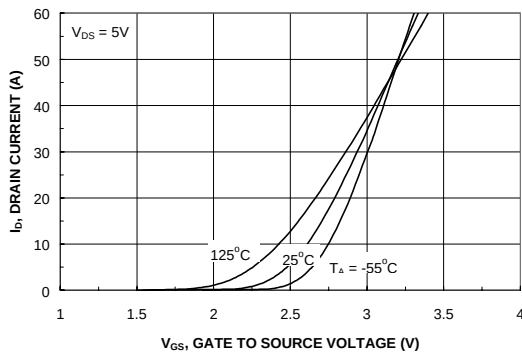


Figure 5. Transfer Characteristics.

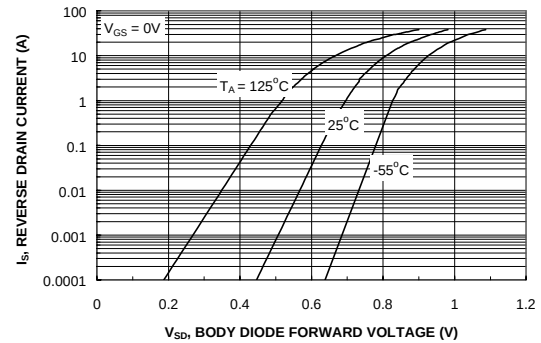


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

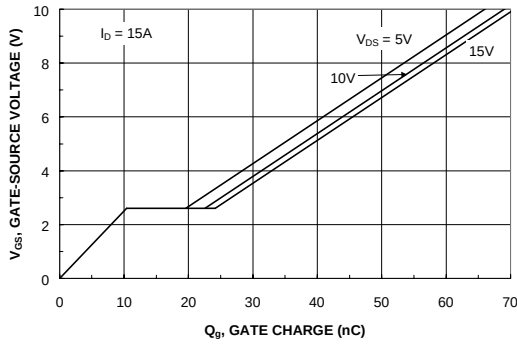


Figure 7. Gate-Charge Characteristics.

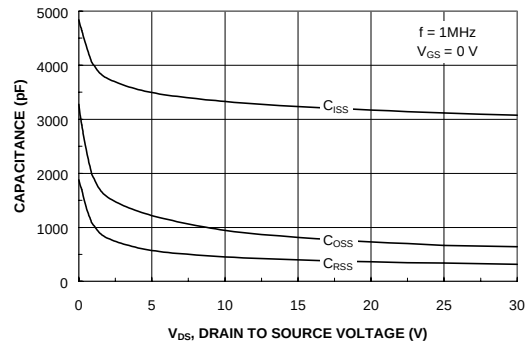


Figure 8. Capacitance Characteristics.

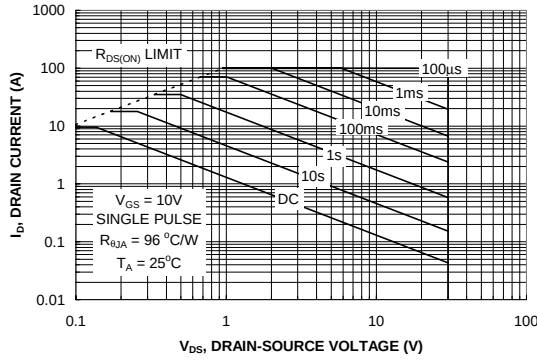


Figure 9. Maximum Safe Operating Area.

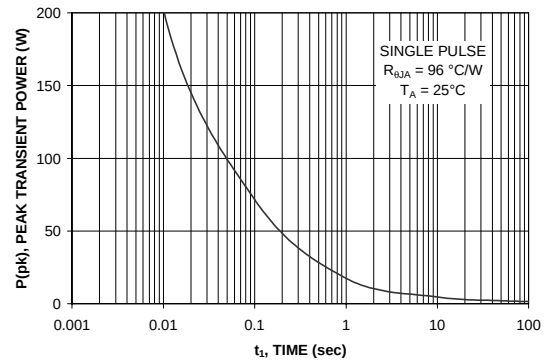


Figure 10. Single Pulse Maximum Power Dissipation.

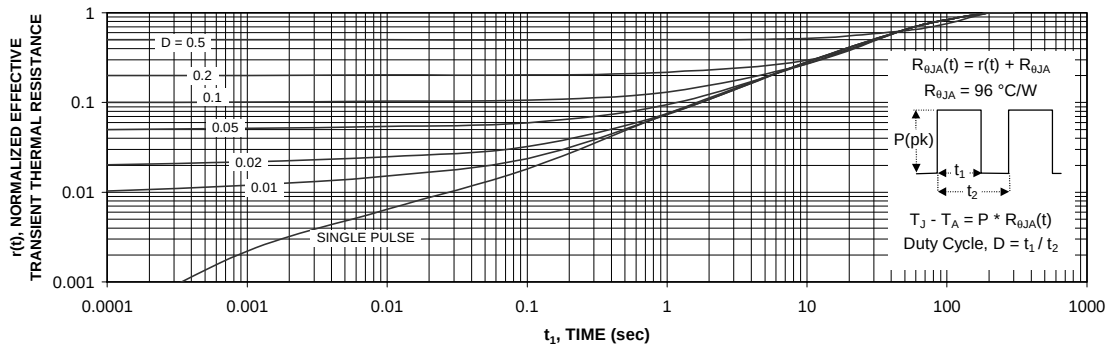


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1.
Transient thermal response will change depending on the circuit board design.

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