

MM54HC151/MM74HC151 8-Channel Digital Multiplexer

General Description

This high speed Digital multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM54HC151/MM74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output high and the Y output low.

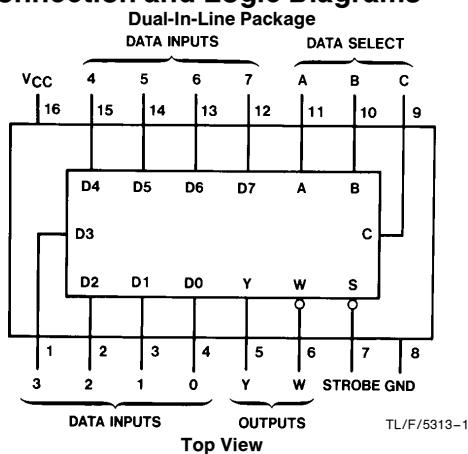
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family.

All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay
data select to output Y: 26 ns
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent supply current: 80 μ A maximum (74HC)
- High output drive current: 4 mA minimum

Connection and Logic Diagrams

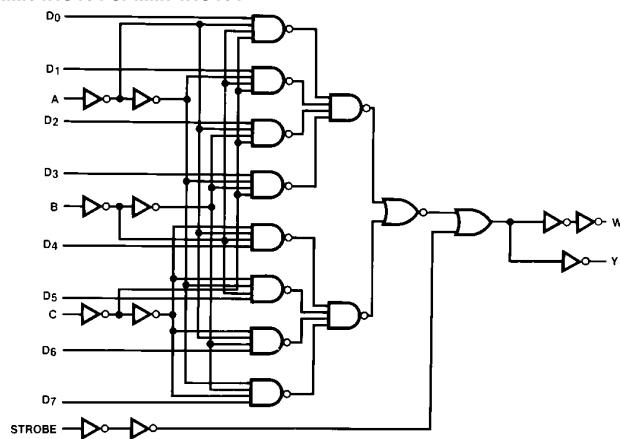


Truth Table

Inputs			Outputs	
Select			Strobe	S
C	B	A	Y	W
X	X	X	H	L H
L	L	L	L	D ₀ \overline{D}_0
L	L	H	L	D ₁ \overline{D}_1
L	H	L	L	D ₂ \overline{D}_2
L	H	H	L	D ₃ \overline{D}_3
H	L	L	L	D ₄ \overline{D}_4
H	L	H	L	D ₅ \overline{D}_5
H	H	L	L	D ₆ \overline{D}_6
H	H	H	L	D ₇ \overline{D}_7

H = High Level, L = Low Level, X = Don't Care
 D₀, D₁...D₇ = the level of the respective D input

Order Number MM54HC151 or MM74HC151



TL/F/5313-2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A) MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	$V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	1000 500 400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		$74HC$	$54HC$	Units
				Typ		$T_A = -40 \text{ to } 85^\circ C$	$T_A = -55 \text{ to } 125^\circ C$	
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V	1.5 3.15 4.2		1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V 4.5V 6.0V	0.5 1.35 1.8		0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0 \text{ mA}$ $ I_{OUT} \leq 5.2 \text{ mA}$	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0 \text{ mA}$ $ I_{OUT} \leq 5.2 \text{ mA}$	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ± 10% the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		24	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		17	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		16	21	ns

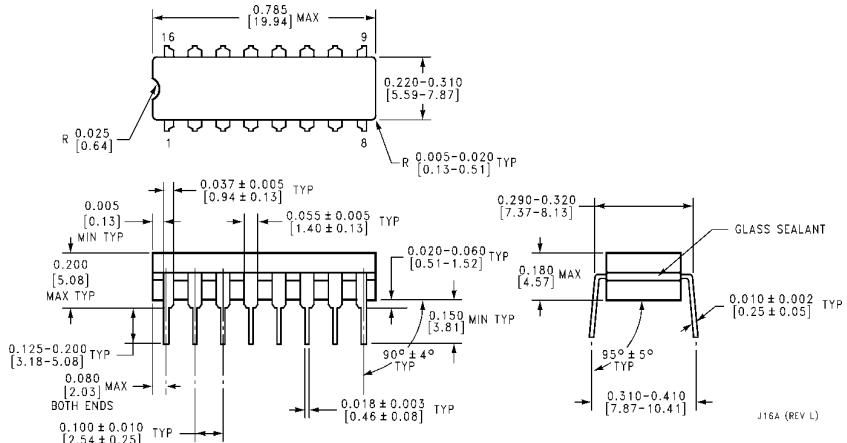
AC Electrical Characteristics $C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		74HC	54HC	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V	90	205	256	300	ns
			4.5V	31	41	51	60	ns
			6.0V	26	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		2.0V	95	205	256	300	ns
			4.5V	32	41	51	60	ns
			6.0V	27	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to Y		2.0V	70	195	244	283	ns
			4.5V	27	39	49	57	ns
			6.0V	23	33	41	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		2.0V	75	185	231	268	ns
			4.5V	29	37	46	54	ns
			6.0V	25	32	40	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		2.0V	50	140	175	203	ns
			4.5V	21	28	35	41	ns
			6.0V	18	24	30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		2.0V	45	127	159	185	ns
			4.5V	20	25	32	37	ns
			6.0V	17	22	28	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

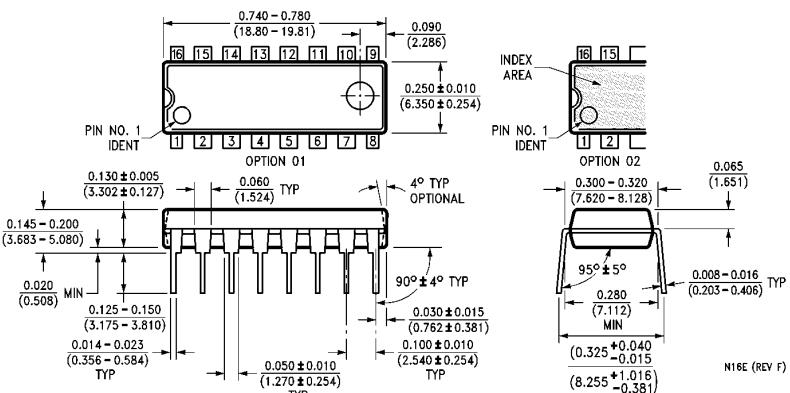
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

MM54HC151/MM74HC151 8-Channel Digital Multiplexer

Physical Dimensions inches, (millimeters)



**Order Number MM54HC151J or MM74HC151J
NS Package J16A**



**Order Number MM74HC151N
NS Package N16E**

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